A review of recent phase change memory developments

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ABSTRACT

Since Stan Ovshinsky's patent filing in 1961 on phase change memory and switching devices [1], there has been a steadily growing interest in this memory. Intel and IBM now consider it competitive with FLASH and DRAM [2,3].

There are numerous other two terminal, nonvolatile, memory technologies competing with it. This talk will examine their market readiness by comparing them to the 50-year development of PRAM.

Key words: Ovonic, PRAM, 3D memory, threshold switching

1. INTRODUCTION

In 1955 Stan Ovshinsky began pursuing new switching materials to implement his ideas in machine control by neuron-like intelligence [4,5]. His most notable achievement in this early work was the development of a TaOx electrolytic switching device he called the Ovitron [6]. He went on to make solid-state versions of this, calling them the "Ovonic Threshold Switch" and the "Ovonic Memory Switch" [7]

Now, 55 years later, this technology is being manufactured and is heralded as the first "Storage Class Memory" [2]. However, it still doesn't have an established market base and many competitive technologies are being pursued in the hopes of beating it to the market.

This paper will consider the requirements for storage class memory and the readiness of the various competitive technologies with respect to PCM. I believe this could shed light on the requirements of a new material technology and why it takes so long to introduce something new.

2. THE LONG DEVELOPMENT CYCLE OF PRAM

Early work in PRAM development occurred at Energy Conversion Laboratories in the early 1960's where the material properties of over 1000 alloys of threshold switching and memory materials were investigated, and suitable contact materials for devices were identified. Widespread interest in this technology began with the publication in Phys Rev Letters of a description of the devices [8]. This interested Intel Corporation, that introduced a 256-bit SRAM (the 3101) and a 1K ROM (the 3301) in 1968. Intel was committed to producing a programmable, nonvolatile product as well and in 1970 developed a 256 bit Phase Change Memory along with ECD [9]. However, with Intel's patent on the EPROM in 1972, they chose to manufacture the 256 byte 1702 EPROM instead.

Energy Conversion Devices went on to produce logic and memory devices without any use of transistors, including an OTS isolated memory array in 1970 [10,11]. In 1986 an integrated 16K bit X 2 layer monolithic 3D memory device was produced at ECD.

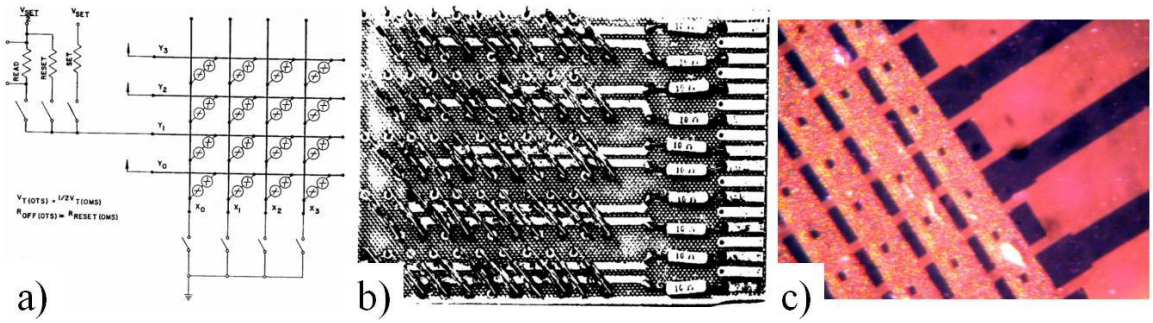

Fig. 1. a) Schematic of the first OTS isolated PRAM b) Photo of the memory c) Integrated array, 2 level memory from 1986.

Work on these devices continued steadily, but the memory suffered from low set speed and high reset current. It was not competitive with the rapidly scaling CMOS based memories.

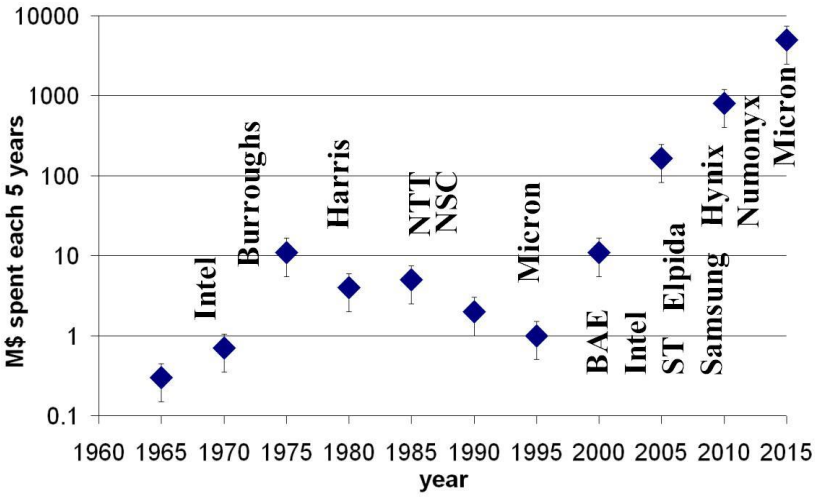

Fig. 2. Estimated investment in PRAM by ECD and licensees

In 1987 IBM and Matsushita developed rapid crystallization alloys for optical disks [12,13]. Based on this work, ECD made fast switching memory devices and continued work on reducing the reset current.

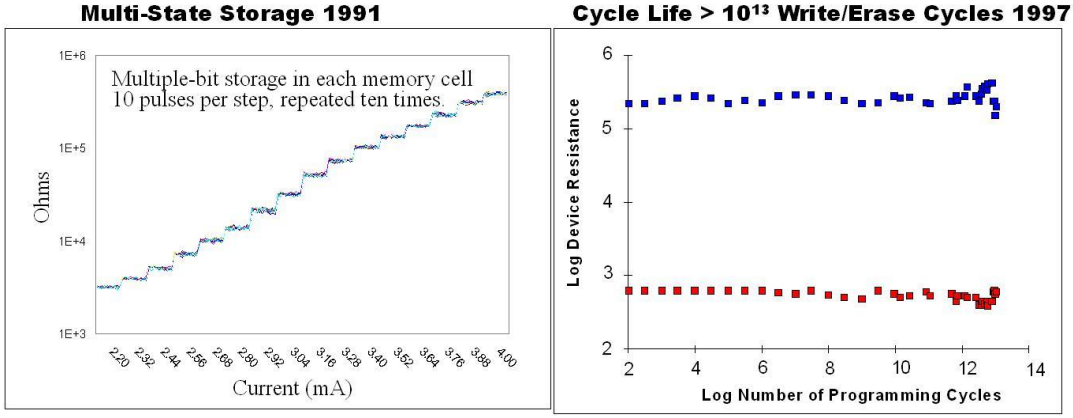

Fig. 3. ECD demonstrations of the potential performance of PRAM

By 1993 ECD had achieved sub-milliamp programming, long cycle life, and multi-level storage that interested Micron, but after making 50nm devices they concluded that the current didn't scale with device area [14]. In 1996, detailed modeling at ECD showed the thermal environment was the most critical factor in achieving low current reset [15] and the devices had to be thermally isolated from the Silicon substrate to work efficiently. Experimental evidence of this convinced former Micron employees to start Ovonyx to commercialize the technology. Ovonyx's partnership with ST yielded the most fruitful results with the successful implementation of a small contact area sidewall electrode [16]. This combined with work on the OTS at Intel resulted in Numonyx developing a practical crossbar memory [17]. Micron acquired all the patents for this technology and will soon be releasing 3D-Xpoint memory [18].

NAND FLASH is approaching the size of 4 square feature lengths per bit. Any new memory technology must also achieve this density to be cost competitive. MOS transistors are difficult to integrate into this size, so other isolation elements are now receiving intensive study. Diodes have issues with leakage and excessive voltage drop. MIM structures have shown some promise, but they have Voltage drop similar to diodes. The Ovonic Threshold Switch is used for isolation in 3D-Xpoint, using an alloy similar to the STAG alloy (Selenium Silicon Sulfur, Tellurium, Arsenic, Germanium) developed by Ovshinsky in the early 1960s [19].

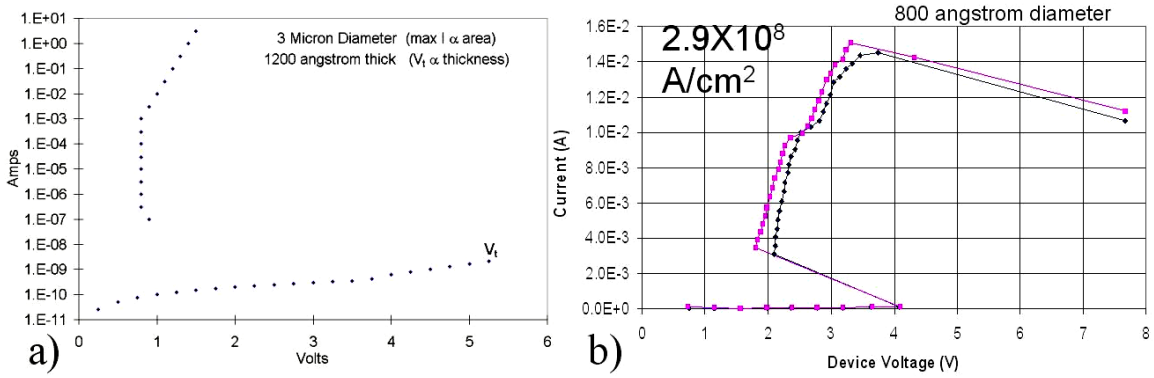

Fig. 4. OTS isolation elements showing: a) On/Off current >1e10 b) high current density

3. COMPETITIVE TECHNOLOGIES

Technology	**PRAM**	**STT-MRAM**	**ReRAM**	**CB-RRAM**	**FeRAM**
Current (uA)	30-100	10	30	10	10
On/Off resistance	1000	3	100	1000	-
Cell Size (f^2)	4	6	4	4	6
Read time (ns)	50	20	50	100	20
Write time (ns)	100	20	50	100	20
Endurance (cycles)	1e9	1e15	1e3	1e3	1e15
Retention time (years)	10	10	.3	.3	1
MLC levels	8-16	2	8	16	2
Switching Energy (pJ)	90	10	90	20	40
Years in development	50	20	10	10	30
Years until Introduced	1-2	3-8	10-15	5-10	10+

Fig. 5. Prediction of Emerging Memory Properties

Numerous 2 terminal, nonvolatile memory devices have been identified and are being pursued as possible candidates for a storage class memory [20,21,22]. These devices could also potentially

benefit from an OTS select element. The table below compares some key parameters of various emerging memory technologies.

IBM has been developing STT-RAM for over 20 years. It has very stable behavior, low switching energy, and the potential to become a 6 square feature size cell. Two drawbacks are the relatively low resistance shift of 2-3X, and the relatively high processing cost of patterning. Preliminary devices show the potential to make a memory nearing SRAM in performance [23]. The development of this technology is comparable to that of PRAM in the 2004 timeframe. However, Samsung and IBM are investing heavily in it and claim products will be forthcoming. STT-MRAM will likely compete with SRAM rather than Storage Class Memory due to cost and density.

Resistive RAM or RRAM devices have a variety of mechanisms, not all clearly understood, that show promise for lower cost, faster speed and lower power nonvolatile memory. Their main drawbacks are that they are not very mature, have short lifetimes, and suffer from retention issues. ReRAM devices work by moving Oxygen or metal ions in an insulating layer. These are being widely investigated but they suffer from short cycle life and process variability [24,25].

Conductive bridge RRAM, called CBRAM is of interest because of the low operating power required. They exhibit better control than ReRAM devices, but when operated with lower power they exhibit poor data retention. [26].

Ferroelectric memory has been pursued for a very long time, but hasn't been successful because of chemical incompatibility of the perovskite materials used and difficulties with scaling. Doped Hafnium Oxide based ferroelectrics have recently been shown to overcome these shortcomings [27].

4. CONCLUSION

Phase change memory is the only emerging nonvolatile memory technology presently being made for storage class memory. Due to the money and time it takes to develop such a product, its lead will be solidified in the next several years. Computing is facing an increasing need for Storage Class Memory to bridge the speed gap between slow memory of disk and SSD and fast memory of SRAM an DRAM. PRAM will be the first new memory technology to bridge this gap. Large investment will continue in this area and other emerging memories will undoubtedly show some superior properties, but the cost of introducing a new memory technology is high.

REFERENCES

1. S. Ovshinsky, U.S. Patent # 3271719, "Resistance Switches and the Like".
2. "Introducing Intel Optane technology bringing 3D Xpoint memory to storage and memory products," Intel News Release, July 23, 2015. (https://newsroom.intel.com/press-kits/introducing-intel-optane-technology-bringing-3d-xpoint-memory-to-storage-and-memory-products/).
3. "IBM Scientists Mark New Advances in Phase-Change Memory", *EE times*, May 20, 2016 (http://electronicdesign.com/memory/ibm-scientists-mark-new-advances-phase-change-memory).
4. S. Ovshinsky, "Nerve Impulse", Communication with Neurophysiology Department, Wayne State University, Detroit, MI, pp22. June 15, 1955.
5. L. Hoddeson and P. Garrett, The Man Who Saw Tomorrow: The Life and Inventions of Stanford Ovshinsky, Chapter 5, (Cambridge, MIT Press, to be published in 2017).
6. S. Ovshinsky, How Liquid-State Switch Controls A-C, *Electronics*, August 14, 1959.
7. S. Ovshinsky, U.S. Patent # 3271591, "Symmetrical Current Controlling Device".
8. S. Ovshinsky, "Reversible Electrical Switching Phenomena in Disordered Structures," *Phys. Rev. Lett*, V. 21, no. 20, pp. 1450-1453, Nov. 11, 1968.
9. R. Neale, D. Nelson, G. Moore, "Nonvolatile and reprogrammable, the read-mostly memory is here," Electronics, pp56-60, Sept. 28, 1970.
10. D. Nelson, "Ovonic Device Applications", J. Non-Crystalline Solids, V2, pp528-539, 1970.

11. U.S. Air Force Contract F33615-68-c-1200.
12. K. Rubin et. al., “Phase Transformation Kinetics - The Role of Laser Power and Pulse Width in the Phase Change Cycling of Te Alloys”, *Appl. Phys. Lett.*, v50, #21, pp 1488-1490, 1987.
13. N. Yamada et. al., “Rapid-Phase Transitions of GeTe-Sb2Te3 Pseudobinary Amorphous Thin Films for an Optical Disk Memory”, *J. Appl. Phys.*, v69 #5, pp2849-2857, 1991.
14. NIST Advanced Technology Program, U.S. Contract No. MDA972-92-C-0054, 1995.
15. G. Wicker, “A comprehensive model of submicron chalcogenide switching devices,” Ph.D. Dissertation, Wayne State University, Detroit, MI, 1996.
16. F. Pellizzer et al., “Novel μtrench phase-change memory cell for embedded and stand-alone non-volatile memory applications”, Symp. on VLSI Tech.,.pp 18 – 19, 2004.
17. D. Kau et. al.,”A stackable cross point phase change memory”, *Proc. IEEE IEDM*, pp 617-620, 2009.
18. R. Bez, P. Cappelletti, G.Servalli and A. Pirovanono, “Phase Change Memories Have Taken The Field,” International Memory Workshop, 2013.
19. S. Ovshinsky et. al., U.S. Patent #8148707 “Ovonic threshold switch film composition for TSLAGS material”.
20. M. Marinella, “Assessment for Storage Class Memory”, ITRS, Feb. 2015.
21. A. Chen, “Ëmerging Nonvolatile Memory (NVM) Technologies”, ESSDERC, pp109-113, 2015.
22. G. Sandhu, “Emerging Memories Technology Landscape”, NVTMS, pp1-5, 2013.
23. J. Nowak et. al., “Dependence of Voltage and Size on Write Error Rates in Spin-Transfer Torque Magnetic Random-Access Memory”, IEEE Magnetics Lett., V. 7, March 8, 2016.
24. S. Sills et. al., “Challenges for high-density 16Gb ReRAM with 27nm technology”, VLSI Tech. Dig., T106-7, 2015.
25. S.Sills et. al., “High-density reRAM for storage class memory”, NVTMS, pp1-3, 2015.
26. J. Guy et. al., “Investigation of Forming, SET, and Data Retention of Conductive-Bridge Random-Access Memory for Stack Optimization”, IEEE TED, v62 #11, pp3482-89, 2015.
27. S. Mueller et. al., "HfO2-based FeFET devices", IEEE Trans. Electron Devices, v60 #12, pp. 4199-4205, 2013

BIOGRAPHY

Guy Wicker is an electrical engineer who has focused on Ovonic switch development since 1985 at Energy Conversion Devices. He is now the CEO of Ovshinsky Innovation, where he is actively continuing this work for memory and logic applications.