Demonstration of Phase Change Memories devices using $Ge_2Sb_2Te_5$ films deposited by Atomic Layer Deposition

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1. INTRODUCTION

Phase change memory technology is considered as one of the most promising resistive memory solution. One issue, however, is the high electrical current required to reset the information. Indeed large energies are mandatory for amorphization of the crystalline phase change material. It has been demonstrated that energies can be highly decreased by reduction of the active volume and confinement of the phase change material. To do so, phase change materials deposition route with high filling capacity is needed. Although Chemical Vapour Deposition (CVD) and Atomic Layer Deposition (ALD) deposition techniques can fulfil these requirements, ALD has major advantages such as low temperature deposition method, ability to tune initial atomic layers for high quality interfaces and production of very high conformal stacks. However, such a process is still a challenge for phase change materials such as $Ge_xSb_yTe_z$ (GST). In this work, (i) ALD GST films are processed and characterized and (ii) realisation of phase change memory devices using ALD GST is demonstrated on 200mm wafers [1].

2. MATERIAL AND PROCESSES

ALD GST films were deposited using an alkyi silyl Te compound, $SbCl_3$ and $GeCl_2{\cdot}C_4H_8O_2$ at 75°C using an ASM Pulsar® 2000 ALCVD™ reactor. GST is deposited by repeating binary Sb - Te and Ge - Te cycles.

100 nm thick films were deposited on thermal oxide in order to perform morphological and physical characterization. Film thickness and uniformity were evaluated by X Ray Reflectivity (XRR). Rutherford Backscattering Spectrometry (RBS) and Particle Induced X-ray Emission (PIXE) were conjointly used to determine average composition. Time Of Flight - Secondary Ion Mass Spectroscopy (TOF-SIMS) was performed in order to obtain composition uniformity across the film and contamination level. Crystallization behavior was followed: resistivity and reflectivity were monitored while temperature increases with a constant ramp rate (20°C/mn). Crystal structure was obtained using X Ray Diffraction (XRD) characterization with a Cu-Kα radiation. Films roughnesses were obtained by Atomic Force Microscopy (AFM). Film conformity was tested through deposition in narrow trenches and Scanning Electron Microscopy (SEM) observations. Electrical evaluation of ALD film properties has been done using a simple pillar architecture [9]. 100nm thick ALD GST films were deposited on 300nm wide W plug. Phase change material was capped with TiN and an upper top electrode. To crystallize the GST, a final 200°C anneal under N_2 was performed.

Integrated PCM devices were tested using a complete automated sequence on a specific set-up fully described in [10]. High frequency voltage pulses with various amplitude and duration were applied to evaluate writing and erasing behavior. The sequence has been conducted numerous times to test endurance of the devices.

3. THIN FILM CHARACTERISTICS

Film composition is $Ge_{19}Sb_{19}Te_{45}$ (RBS/PIXE). On 200mm wafers, less than 3% 1σ thickness non uniformity is monitored by XRR. Film roughness is around 1.8nm RMS, before and after 400°C anneals as demonstrated by AFM.

Except at the top surface where film is oxidized, film composition (Ge, Sb, Te) is found uniform across the layer. Cl contamination is detected whereas C and Si level are closed to detection limit.

Evolution of reflectivity and resistivity with temperature are monitored and, at low temperature, for as deposited films, low reflectivity and high resistivity are measured. These values are characteristics of an amorphous GST layer. The amorphous structure is confirmed on the XRD spectrum. When temperature increases, at 147°C, a transition occurs and reflectivity highly increases and resistivity progressively decreases. Note that resistivity varies by four orders of magnitude. As shown by diffraction data, this is the sign of the transition between the amorphous phase and the crystalline face centred cubic (fcc) phase. At 305°C, a slight increase in reflectivity is monitored. This correspond to the phase transition between fcc and

hexagonal compact (hc) $Ge_2Sb_2Te_5$ phase. It is worth noting that this crystallisation behaviour is similar to the one observed for a $Ge_2Sb_2Te_5$ film deposited by classical sputtering [11].

4. MEMORY DEVICES CHARACTERIZATION

The conditions of electrical amorphization of PCM cells were studied: on cells which are initially crystalline (SET state), resistances were measured after voltage pulses of increasing intensity and constant length (100ns). A clear SET to RESET transition is observed: amorphization occurs for pulse generator voltage as low as 2V.

Using these results, it was possible to study RESET to SET transition: a first amophization pulse is carried out. After this amorphization step, a voltage pulse of various intensity and duration is done. Then, resistance is measured. A more complete crystallization is observed for 1000ns long pulses: the resistance variation is higher than one order of magnitude. No crystallization occurs with 25ns long pulses. The 100ns pulses present an intermediate situation.

Finally, the endurance of these PCM cells was investigated: up to 10^6 cycles can be performed with a very stable resistance for SET and RESET states.

5. CONCLUSION

The development and integration of $Ge_2Sb_2Te_5$ thin films deposited by ALD was performed. The layers present the targeted composition, a nice uniformity on 200mm wafers, a low roughness, a high conformity and a classical phase change behavior. As expected, the resistivity variation between the as deposited amorphous layer and the crystalline structure is of 4 orders of magnitude.

Finally, these films were successfully integrated in pillar PCM cells. The cell switching between low resistive and high resistive state was obtained during 10^6 cycles without degradation.

This work demonstrates the feasibility of Phase Change Memory cells using GST deposited by ALD on 200mm wafers.

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Short CV

Sylvain Maîtrejean has been in the staff of CEA Leti (Minatec Campus) since 2000. Within the Silicon Technologies Department, he is the manager of the Advanced Material Deposition laboratory. Before joining LETI, he hold a master's degree in physics and material science at the Grenoble National Engineering School for Physics (ENSPG) in 1996. In 2000, he received a Ph.D. in physical metallurgy from the National Polytechnic Institute of Grenoble (Grenoble-INP).

Within CEA Leti, his first activities involved metallic thin film process and characterization for CMOS devices with special focus on metal gate. Later on, he was in charge of the BEOL integration group and participated to the development of advanced interconnects such as Cu/ULK interconnects, 3D integrated circuit and Carbon nanotube interconnects. His major actual research field concerns the development of material and integration processes for resistive memories. His main research interests are the mechanical reliability of narrow devices and the impact of nano-confinement on microstructure evolutions and materials properties.

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