Phase Change Memory Technology for 90nm Embedded Non Volatile Memory Applications

Roberto Annunziata, Paola Zuliani, Elisabetta Palumbo, Carlo Bergonzoni, Massimo Borghi, G.Dalla Libera and Monica Martinelli
Technology R&D, STMicroelectronics, via C.Olivetti 2, 20041 Agrate Brianza (MI), Italy
Mail to: roberto.annunziata@st.com, paola.zuliani@st.com,

1. INTRODUCTION

While advanced CMOS roadmap is more and more facing low voltage operation and low consumption requirements, basically non-scaling High Voltage devices are needed by conventional Floating Gate memory solutions. With this respect the low voltage operation of Phase Change Memory (PCM) devices, associated with simpler process architecture, makes them particularly appealing for embedded applications. The choice of an MOS selector can guarantee both competitive cell area and low cost process, thanks to very few additional masks needed for storage element definition. In this case a split gate layout (two polysilicon gates connected in parallel) with local interconnection on the source line is considered the most effective solution. The PCM storage element $Ge_2Sb_2Te_5$-based is located on the drain of the select transistor. In this work, results obtained on 90nm ePCM technology in terms of performances and reliability both cell and macrocell level are presented.

2. EXPERIMENTS

Based on 90nm CMOS platform, with 2.1nm Low Voltage, 6.5nm Medium Voltage transistors and 6-ML copper Back-End, a full integration of 4Mb e-PCM macrocell has been obtained [1,2]. Cell architecture is "wall"-like [3] with MOS selector (Fig.1). Non-standard MOS transistor operating conditions are required to keep compact cell area and to sustain high peak current required for PCM programming. Nevertheless, thanks to fast cell programming strong overdrive conditions for MOS selector can safely be guaranteed also for 1M cycling (Fig.2). A TCAD model based on a 3D description of the system has been developed for e-PCM cell engineering. Comparison with experimental data has shown good agreement and predictive capabilities. Optimized cell working point has been studied by means of TCAD simulations, including the MOS select transistor and the storage element up to first metallization level. Materials constituting the storage element are treated as conductors, whose physical, electrical and thermal properties are well known [4]. Finally, data retention capability of ePCM memory array, once integrated on a 6-ML advanced CMOS platform, has been studied both at cell and macrocell level by considering the impact of different storage temperatures.

3. RESULTS & DISCUSSION

In order to optimize cell working point in the memory array, an evaluation of best conditions for MOS select transistor polarization has been carried out (Fig.3). By considering different heater resistivity (in the range of 1-5kΩ series resistance) and increasing values of applied Word Line voltage, an optimal working point can be identified in the I-V plot for the Bit Line in programming conditions. Limitations on maximum Bit Line voltage are defined by design, while Word Line voltage constraints are related to MOS reliability during cycling. No issues related to thin oxide degradation have been observed with voltages up to 3V on selector gate (unselected BL) and on selector drain (unselected WL), thus defining a specific target area in the I-V plot of Fig.3. Specifications for embedded non-volatile memory applications such as Smart Cards and industrial microcontrollers rely on consumer range (-25…85C). Data retention evaluation on fully integrated memory elements has been carried out both cell and macrocell level (Fig.4-5). 1ppm defectivity-level for tail bits of Reset distribution has been considered the failure criterion at Read0 conditions. Corresponding resistivity value has been used for time to failure evaluation at different temperatures on analytic cell. Activation energy values in the range 2.6-2.9eV have been obtained both cell and macrocell level. Same kinetic is then expected for tail bits and for median of distribution. In case of worst case bits (macrocell data), extrapolation at 10 years data retention gives 100C temperature, so ensuring margin for target embedded applications.

4. CONCLUSION

For the first time the PCM storage element has been successfully integrated in a 90nm 6-ML advanced CMOS platform, with definite advantages in terms of process simplicity and costs with respect to conventional non-volatile memory approaches. Macrocell-level competitive performances in reading and writing have been demonstrated. A powerful TCAD simulation tool has been developed for cell performances and working point optimization. Finally, an

extended data retention study has been carried out on multi-megabit ePCM array with several Gb statistics, showing that consumer range specification are satisfied with margin.

Acknowledgements

The authors would like to acknowledge colleagues in Numonyx R&D for valuable support during all the stage of technology development.

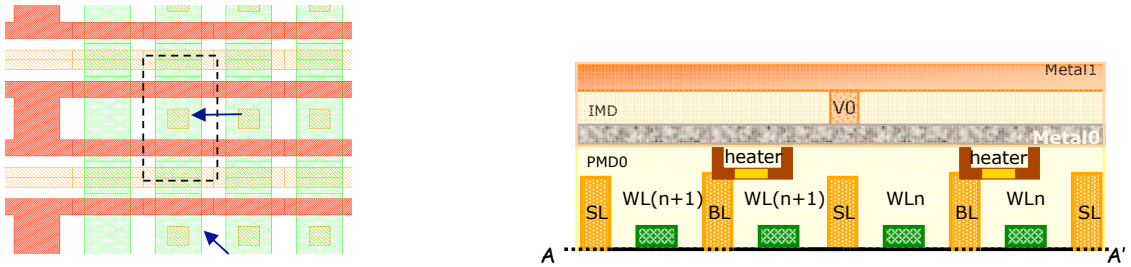
REFERENCES

[1] R.Annunziata et al. "Phase Change Memory Technology for Non Volatile Memory Embedded Applications for 90nm and Beyond", IEDM Tech.Dig., 2009

[2] G.De Sandre et al. "A 90nm 4Mb Embedded Phase-Change Memory with 1.2V 12ns Read Access Time and 1MB/s Write Throughput", ISSCC 2010

[3] R.Bez "Chalcogenide PCM: a Memory Technology for next Decade", IEDM Tech.Dig., 2009

[4] C.Wiemer, "Chemical vapor deposition of chalcogenide materials for phase change memories", Proc. of International Workshop on Emerging Non Volatile Memories, 2007



(a) (b)

Fig.1 Schematic layout of the MOS-selected PCM cell (a) and cross section along Bit Line direction (b). Two transistors in parallel address the same storage element and common source is biased by local interconnect.

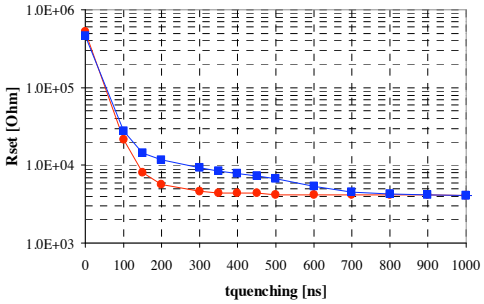


Fig.2 Set level as function of trailing pulse length on analytic cell. Degradation in Set performances is due to not optimized heater-precontact interface (blue curve).

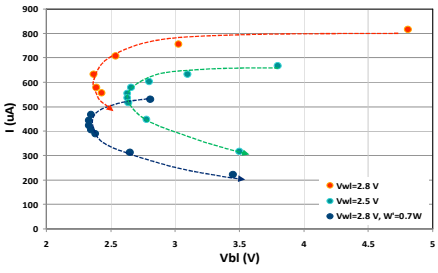


Fig.3 Cell working point optimization (TCAD results). Expected programming current as function of Bit Line voltage is reported at different Word Line voltage (2.5-2.8V) by varying heater resistivity. Constant dissipated power is considered.

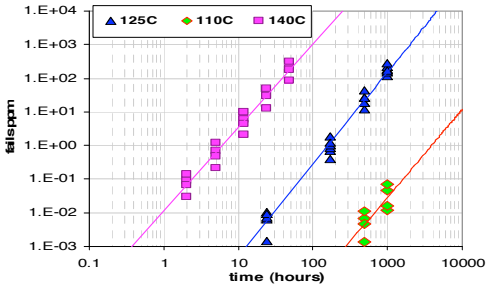


Fig.4 Data collection for activation energy evaluation. Kinetic of tail bits on 4Mb ePCM macrocell at three different temperatures has been followed.

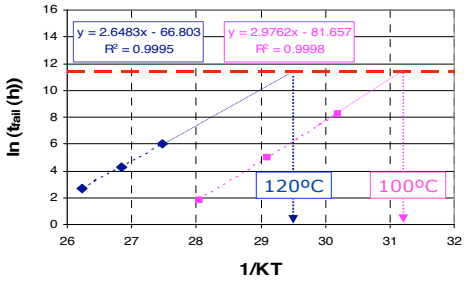


Fig.5 Evaluation of activation energy for crystallization, based on analytic cell (blue) and macrocell (pink) data.