Ti Impact in C-doped Phase-Change Memories compliant to Pb-free soldering reflow

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ABSTRACT

In this paper, we investigate the performances of carbon-doped Ge2Sb2Te5 films (named hereafter GST) which have been integrated together with a thin titanium capping layer into Phase-Change Memory devices. We show that the carbon content into GST and the titanium cap layer thickness can be optimized to obtain an Amorphous As-Deposited (A-AD) phase which is stable under both the typical Back End-Of-Line (BEOL) thermal budget (2 min at 400 °C) and standard Pb-free soldering reflow process conditions (temperature peak at 260 °C). Therefore, the material obtained at fab-out keeps its disordered phase and can be used to pre-code one state of information stable against the standard soldering reflow (peak at 260 °C). We propose to use this high resistance state together with an electrically induced low resistance state to pre-code the memory prior to PCB manufacturing.

Key words: reliability, phase change memory, Carbon-doped GST, soldering issue.

1. INTRODUCTION

Phase Change Memories PCM, which rely on the change of the crystalline phase of a chalcogenide compound, are today considered as an emerging rival for embedded Flash memories. Nevertheless, their industrialisation still faces some challenges [1], such as increasing the thermal stability of the two memory states. In this context, we highlight here a PCM stack offering a high thermal stability of the Amorphous As-Deposited (A-AD) state. We show how the optimisation of the carbon content introduced into GST and Ti cap thickness allows obtaining an A-AD material which is robust toward a 2min @400°C BEOL-like thermal anneal. We then demonstrate how the post BEOL annealed amorphous cells can be pre-programmed into the crystalline SET state by a specific electrical pulse sequence, and how the pre-coded information is hereafter preserved throughout the soldering reflow process.

2. DESCRIPTION OF THE MEMORY CELL STRUCTURE

Carbon doped GST thin films of thickness 100nm were fabricated by co-sputtering using two targets, namely GST and pure Carbon. The C content was tuned between 0 and 15 at%. A thin Ti cap layer was introduced on the GSTC layers ranging on 0, 5, 10nm. The bilayers GSTC/Ti were integrated in the analytical cell schematically presented in Fig. 1. The bottom electrode contact of the lance-type structure consists of a tungsten plug of diameter 300 nm.

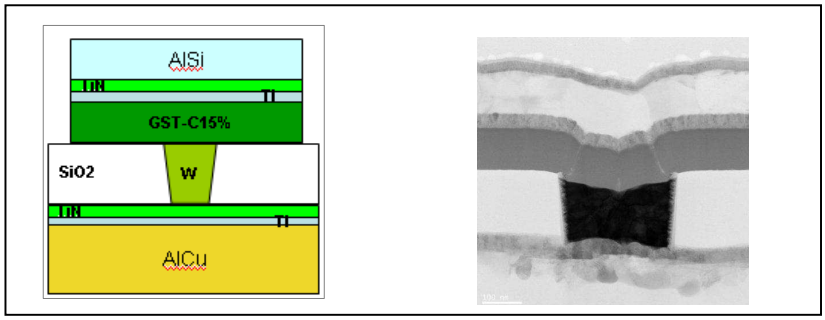

Fig 1: Simplified schematic and TEM picture of the plug Phase-Change-Memory structure based on GST-C15% with titanium top layer. The TEM picture shows the interface between the phase-change material (GST-C15%) and the titanium layer.

3. MATERIAL CHARACTERIZATION

A. Effect of carbon additions into GST:

Resistivity measurements have been performed as a function of the temperature on as-deposited carbon-doped GST thin films, with carbon contents ranging from 0 to 15 at.%. Fig. 2 shows that the crystallisation temperature Tx increases with the carbon content, and reaches up to 350°C with 15at% carbon.We conclude that the thermal stability of the amorphous as-deposited GST-C film is strongly improved with the addition of carbon.

This result can be explained by the formation of strong bonds into the chalcogenide material GST-C when subjected to high thermal stress [2]. Indeed, the carbon element tends to create C chains or to bind with Ge. Consequently, the crystallization speed is slowed down due to carbon doping and the crystallisation temperature is increased, as demonstrated in the literature [4].

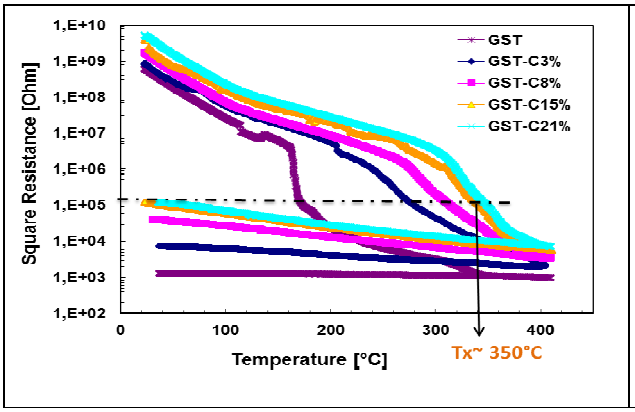

Fig 2: Resistivity measurements as function of temperature for different carbon contents in GST thin films. Carbon doping allows boosting Tx near BEOL thermal budget.

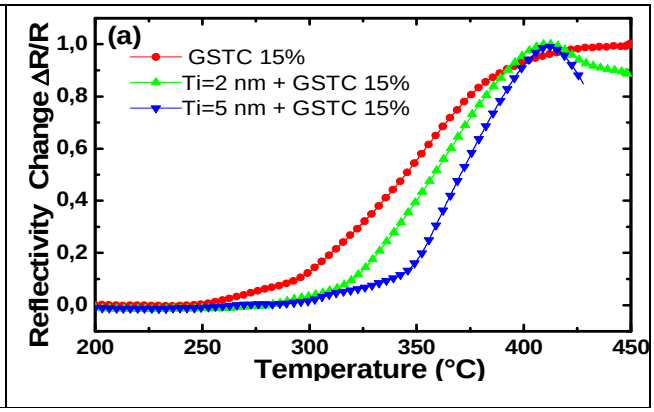

Fig 3: Reflectivity vs temperature of GST-C15% with different deposited Ti capping layer. The crystallization is slowed down due to Ti cap and the titanium layer.

B. Effect of the Ti cap thickness:

Titanium is a key material commonly used to ensure proper adhesion between layers [3]. In the case of PCM devices, it improves the adhesion to the top electrode through the formation of Ti-Te bonds [2], [3]. We have characterized the effect of introducing a thin Ti cap layer on the GST-C layer.

The reflectivity measurements performed for various titanium cap thickness (Fig. 3) show that the crystallisation temperature is further increased with the introduction of the Ti cap. The combination of 15 at.% carbon and a 5nm Ti cap layer results in an increase of the crystallization temperature of ~ 40 °C which closely approaches the BEOL annealing temperature.

The origin of the improved thermal stability of the films following the introduction of carbon into GST and the use of a thin Ti cap has been investigated with a local composition analysis of our analytical cells. The elemental composition cartographies obtained by EELS for Ti, Te, C and Sb (Fig.4) on GST-C15%+ Ti=5nm devices show several features after the 400°C BEOL annealing.

The device comprising the Ti cap layer reveals a diffusion of Ti toward the phase-change film. In this case, Ti diffusion is accompanied by a non homogeneous distribution of Te and carbon along the thickness axis of the phase change film, while the Sb distribution is shown to remain homogeneous. Fig. 4 reveals the enrichment in Te when going toward the Ti cap and in the opposite direction the enrichment in carbon toward the W plug. As a result, we expect this high carbon content region to have an improved thermal stability as revealed by the materials characterization, leading to a delayed crystallization process and an improved thermal stability of the amorphous as-deposited phase.

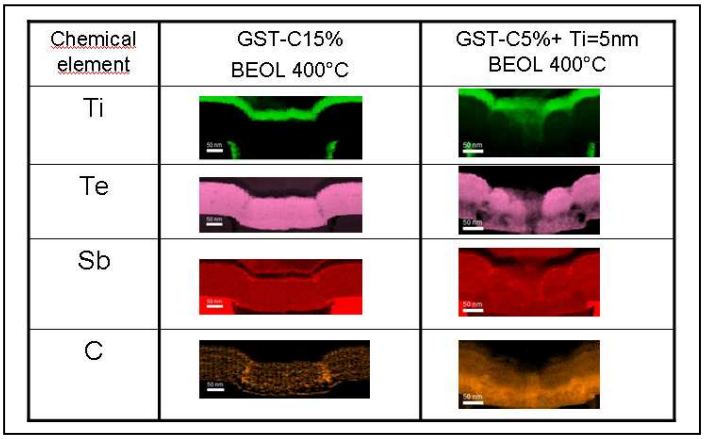

Fig 4: Elemental composition cartographies obtained by EELS Microscopy for Ti, Te, C and Sb elements on GST-C15% show several features after BEOL: With Ti capping layer, migration of elements is observed and two regions are formed, Ti-Te rich region near the top electrode and Ge-C rich region near the bottom electrode. This high carbon content region allows improving the thermal stability of the A-AD phase.

4. ELECTRICAL CHARACTERIZATION

A. Programming performances

Next we present the programming characteristics of the analytical cells displayed on Fig. 1, with a focus on the devices including a 15 at.% carbon doping into GST plus a 5nm Ti cap layers. Standard GST devices were also characterized for reference. All the fabricated devices have undergone a 2min at 400°C BEOL-like anneal prior to electrical testing, bringing them into the so-called BEOL state. The BEOL state of the GST reference devices is a low resistance state, since the devices have crystallized at a temperature close to the crystallization temperature of 150°C. On the contrary, because of the high thermal stability of the stack including 15 at.% C doping and the 5 nm thick Ti cap layer (Fig. 3), the BEOL state of the corresponding analytical cells is a high resistance state, since the phase change material remains amorphous throughout the fabrication process and BEOL anneal.

Fig. 5 shows the programming characteristics of the GSTC15% devices including a 5nm thick Ti cap, as compared to standard GST devices. As already foreseen in the resistivity measurements (Fig. 2), the dynamic electrical results confirm that carbon doping reduces the crystallisation speed: pulses longer than 1000ns are required to obtain a resistance contrast of more than 1 order of magnitude, while GST devices are programmed with 100ns pulses with a contrast of more than 2 orders of magnitude. A **SETMIN procedure** was developed to bring the devices to a state of minimum resistance value. It consists in 5 pulses with the following characteristics [4V, rise 1µs, width 10µs, fall 10µs].

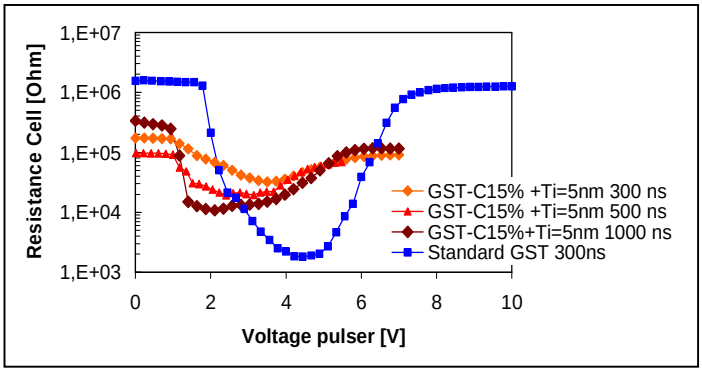

Fig 5: Programming characteristics of GST-C15%+ Ti= 5nm devices obtained with different pulse width (300ns, 500ns and 1000ns). The Comparison between the programming curves of GST-C15%+ Ti= 5nm and standard GST after BEOL thermal budget shows that carbon doping reduces both the crystallisation speed and the resistance contrast between the SET and RESET states.

The programming characteristics after the SETMIN procedures are shown to exhibit a **reliable** programming behaviour, with resistance window between the SET and RESET states of more than 1 order of magnitude. Besides, no significant modifications of the SET and RESET programming currents are observed versus the initial state of the device and **both the BEOL and SETMIN states demonstrate a reduction of ~30% of the reset current** as compared to the standard GST reference [4]. Endurance tests, where the devices are submitted to a sequence of alternative set and reset pulses, demonstrated a cyclability of more than 10^8 cycles, with no degradation of the resistance window.

B. Robustness against soldering reflow:

The method we propose to solve the soldering issue of the PCM relies on the high thermal stability of GSTC15%+Ti=5nm. We can pre-code two states of information on the BEOL devices using the SETMIN procedure.
Indeed, the BEOL state can be used as a first state of information, being a high resistance state. Desired cells can then be programmed to a low resistance state by the suitable SETMIN electrical procedure. Fig. 5 exhibits the standard drift behaviour of the BEOL and SETMIN states. The low value of the drift coefficient (ν<0.1) will allow maintaining a suitable resistance contrast between the two states over time so that the pre-coded information can easily be re-covered. We finally demonstrate that the contrast of more than 1 order of magnitude between the resistance value of the BEOL and SETMIN states is also maintained after emulating a soldering reflow temperature profile (peak @ 260°C) on the devices (Fig. 6).

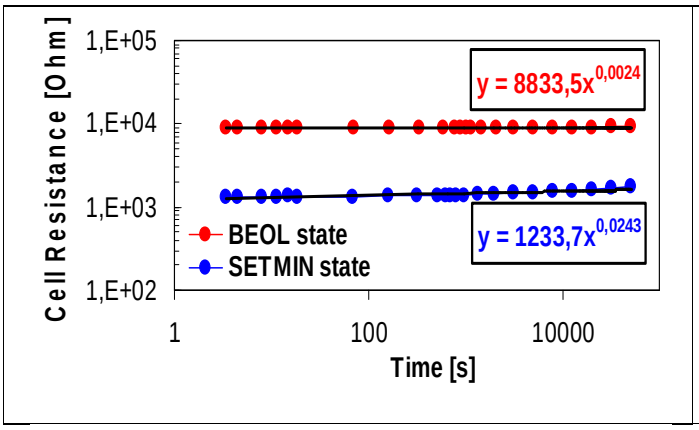

Fig 5: Graphs showing the thermal stability of the two coded states: BEOL annealed cells and SETMIN state cells.

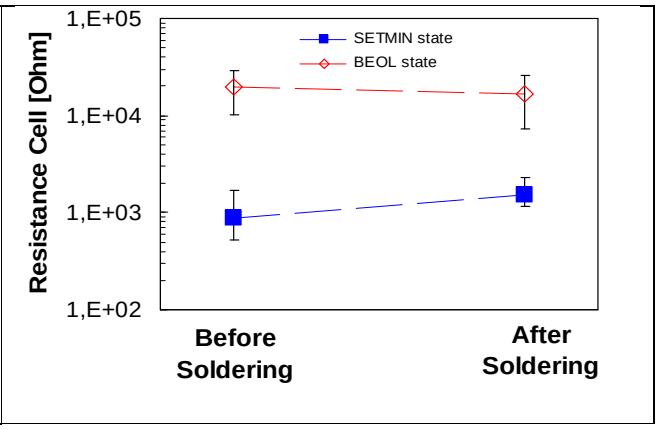

Fig 6: Resistance levels of the two coded states (the BEOL and SETMIN states) before and after soldering. One decade of resistance is kept between the two kinds of coded cells after the soldering reflow temperature profile

5. CONCLUSION

In this paper, we have shown that a carbon doped GST based devices comprising a thin Ti cap is able to sustain both the BEOL-like anneal and the soldering reflow profile while remaining in a highly resistive amorphous state. We have proposed a specific electrical procedure to program the devices into a low resistance crystalline state which is maintained throughout the soldering operation. The combination of our optimised stack with a suitable programming procedure allows then pre-coding the information at wafer level prior to PCB manufacturing.

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