Predicting the performance of electrical probe storage on phase-change media

Mustafa M. Aziz, and C. David Wright[1]
School of Engineering, Computer Science and Mathematics, University of Exeter, Harrison Building, Exeter EX4 4QF, United Kingdom

ABSTRACT

Very high-density data storage has been demonstrated using nanoscale electrical probes with phase-change media. In this technology, an electrically conductive probe is brought in contact or in proximity to a phase-change structure to pass a sufficient current to induce irreversible amorphous or crystalline transformations in the form of dots to record information. This work develops an analytical theory of contact recording by probe of phase-change media to derive expressions for the threshold voltage, expected dot sizes and amorphous-to-crystalline transition lengths as functions of the system geometry and dimensions and material properties. The theory is shown to be in good agreement with published experimental measurements and shows explicitly the interrelation between the various parameters in these systems.

Key words: probe storage, phase-change media, electrothermal model.

1. INTRODUCTION

Towards the achievement of increased data storage densities, memory devices incorporating probes have been suggested. These devices borrow the existing nanoscale resolution found in Atomic Force Microscopy (AFM) and its derivatives to record data bits on storage media. One approach, which is the focus of this paper, involves using electrically conductive probes in contact with phase-change media to pass a current that raises the temperature in the phase-change layer and induces semi-permanent phase transformations to store data as amorphous or crystalline dots. Crystalline dot sizes as small as 50 nm were recorded experimentally in thin-films of amorphous material [1–4] with areal densities approaching 1 T/in^2 indicating the promise of this technique for high density data storage. The crystalline phase is characterised by high electrical conductivity, while the amorphous phase is characterised by low electrical conductivity. Hence on reply, a small voltage is applied across the phase-change layer producing variations in the sense current of the probe as it scans regions of differing conductivities in the phase-change layer.

The recording process in these systems is complex and involves thermal, electronic and kinetic processes that, along with the system's geometry and dimensions, ultimately determine the size and shape of the recorded dots. Numerical simulations using the finite element method were therefore performed to model the record and erase processes to enable the design of an efficient material structure and to understand the factors that determine the size and shape of recorded dots [5, 6]. This work aims at producing simplified analytical models that explicitly show the dependence of the threshold voltage, dot sizes, and amorphous-to-crystalline transition lengths on the material parameters and system geometry and dimensions. In doing so, the theory is developed at one particular temperature at which an irreversible amorphous-to-crystalline transition takes place - called the transition temperature. The temperature and electric field dependencies of the electrical conductivity of the phase-change layer from room temperature leading up to this transition temperature is therefore not included in this theory, but nevertheless is implied through the value of the electrical conductivity at the transition temperature obtained from measurements.

Section 2 of this paper describes a simplified electrothermal model of a basic two layer phase-change structure that is later used in section 3 to estimate the required threshold voltage for crystallisation and the resulting dot sizes. In section 4, the slope theory is used to estimate the extent of the amorphous-to-crystalline transition and outline the requirements for minimising its length.

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[1] Authors emails: M.M.Aziz@ex.ac.uk
David.Wright@ex.ac.uk

2. ELECTROTHERMAL MODEL

Figure 1 shows a diagram of the two dimensional probe system that is modeled with L being the tip contact length with the material, and δ_p and δ_u are the thicknesses of the phase-change layer and underlayer respectively. The thickness of the substrate is assumed to be much larger than the phase-change layer and underlayer. The tip is represented by an infinitely conducting semi-infinite block maintained at positive potential +V with respect to the high conductivity underlayer which is held at zero potential. The storage medium structure consists of a phase-change or recording layer on top of an infinitely conducting underlayer as the return electrode, which is deposited on a substrate.

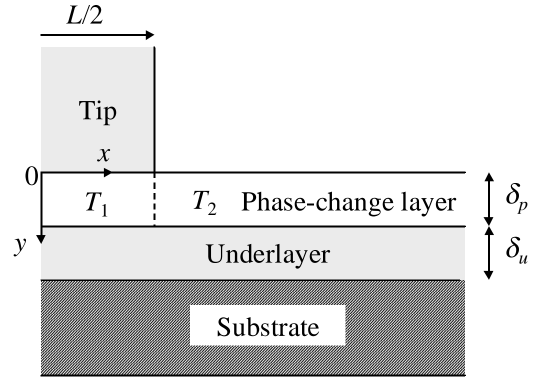

Fig. 1 Geometry of modelled recording system.

The temperature distribution in the phase-change layer can be determined from the steady-state heat conduction equation for this system which is given by [7]:

$$\frac{\partial^2 T}{\partial x^2} - G(T - T_o) = \frac{-P}{k_p} \tag{1}$$

where T represents the thickness averaged temperature in the phase-change layer, T_o is the ambient temperature (equal to 293 K here) and $P = \sigma_p|\boldsymbol{E}|^2$ is the power density of the heat source, produced by the tip-underlayer electric field $\boldsymbol{E}$ in the phase-change layer of electrical conductivity σ_p. The coefficient G (with dimensions m^{-2}) is given for the system shown in Fig. 1 by [7]:

$$G = \frac{1}{k_p \delta_p}\left[H_t + \frac{H_b}{1 + H_b(\delta_u / k_u)}\right] \tag{2}$$

where k_p and k_u are the thermal conductivities of the phase-change layer and underlayer respectively. The thermal coefficients H_b and H_t at the interface between the underlayer and substrate and at the top of the phase-change layer respectively, can be used to study the influences of different substrate material, different coating material and finite heat flow through the tip on the temperature distribution in the phase-change layer.

For a thin phase-change layer, the factor G becomes large and (1) may be written, to a good approximation, as [7]:

$$T - T_o \approx \frac{-P}{Gk_p} \tag{3}$$

Equation (3) will be used in the following sections to derive expressions for the voltage required to induce irreversible amorphous-to-crystalline transition and to for the expected size of recorded bits.

The source of heat energy is Joule heating resulting from current flow in the phase-change layer induced by the electric field distribution between the tip and the underlayer. This field can be determined from solution of Laplace's equation $\nabla \cdot \boldsymbol{E} = 0$. Assuming that the y-component of the electric field is dominant, the approximate analytical solution to Laplace's equation was found to be [7]:

$$E_y = \begin{cases} E_o, & -L/2 \le x \le L/2 \\ E_o \dfrac{d}{d + 2\delta_p(|x| - L/2)}, & |x| > L/2 \end{cases} \tag{4}$$

where $d = \pi y(2\delta_p - y)$, $y = \delta_p/2$, $E_o = V/\delta_p$ and V is the applied tip voltage.

It will be assumed in this work that there is negligible heat flow through the tip and hence surface of the phase-change layer is thermally insulated. This leads to a bell shaped temperature distribution in the phase-change layer peaking at the centre of the coordinate system in Fig. 1. Finite heat flow through the tip can be shown theoretically to lead to temperature maxima occurring at the corners of the tip, and an overall reduction in the temperature of the phase-change layer.

3. THRESHOLD VOLTAGE

During crystallisation, the temperature in the amorphous phase-change layer is raised by the passage of current from the tip to the underlayer. Provided that the temperature increases beyond a threshold value T_t, referred to here as the transition temperature, an irreversible amorphous-to-crystalline transformation will take place in the heated region accompanied by an increase in the electrical conductivity. The voltage required to be applied to the tip to reach the transition temperature is called the threshold voltage and represents the minimum voltage required for an irreversible transformation and leads to the smallest crystalline dot size. This voltage can be estimated from (3) using the electric field directly underneath the tip defined in (4) in the region $-L/2 \le x \le L/2$ and is given by:

$$V_t = \delta_p \sqrt{\frac{k_t G(T_t - T_o)}{\sigma_t}} \qquad (5)$$

where k_t and σ_t are the thermal and electrical conductivities at the transition temperature. It can be easily shown that after substitution of G from (2) into (5) that the threshold voltage has a square root dependence on the thickness of the phase-change layer as found experimentally [3] and shown in Fig. 2.

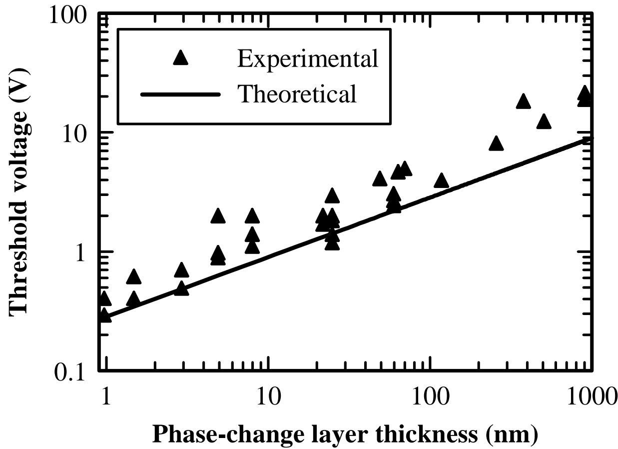

Fig. 2 Calculated thershold voltage compared with measured values from ref. [3].

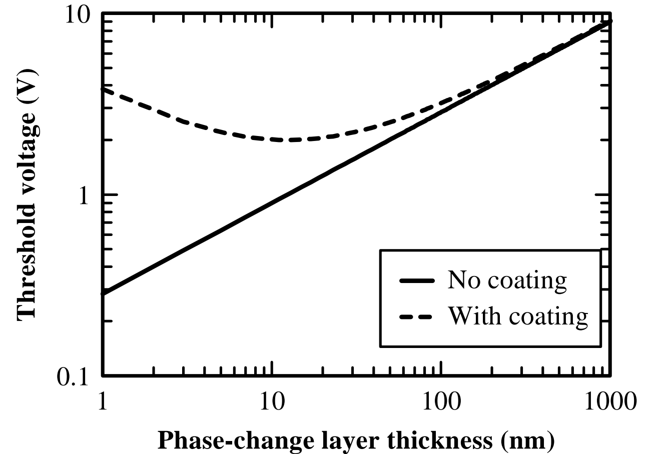

Fig. 3 Influence of coating layer on the threshold voltage as a function of phase-change layer thickness.

Figure 2 compares equation (5) with published experimental measurements of threshold voltages on thin-films of $Ge_2Sb_2Te_5$ phase-change material [3] having thicknesses 1 - 900 nm on top of 20 nm Au-Ni underlayer, and finally deposited on oxide glass substrate. The phase-change layer was coated with a protective liquid that can be considered as a good thermal and electrical insulator. The constant writing voltage was applied, through a series resistor, to either an Au-Ni coated tip or a sharpened Au wire in contact with the phase-change layer. The threshold voltage was recorded as the voltage that causes irreversible electrical switching. The phase-change material properties used in

equation (5) are listed in Table I, the thermal conductivity of the gold underlayer was taken to be 50 W/(mK), and a thermal coefficient of 2×10^8 W/(m^2K) as assumed at the Au-Ni/glass interface (typical value for a dielectric/metal interface [8]). Good agreement can be observed in Fig. 2 between the measured and theoretical values of threshold voltages, demonstrating the predicted square root dependence on thickness of the phase-change layer.

TABLE I. Thermal and electrical properties of $Ge_2Sb_2Te_5$ used in the calculations. Subscripts (c), (a) and (t) denote values at the crystalline phase, amorphous phase and at the transition temperature respectively. *k* is the thermal conductivity, and σ electrical conductivity of the phase-change material.

Symbol	Value	Units
T_t (1.6K/min)	428[a]	K
k_c (300K)	0.53[b]	W/(mK)
k_a (300K)	0.24[b]	W/(mK)
k_t (428K)	0.4	W/(mK)
σ_c (300K)	3250[c]	$(\Omega m)^{-1}$
σ_a (300K)	0.4[c]	$(\Omega m)^{-1}$
σ_t (428K)	310[c]	$(\Omega m)^{-1}$

[a]Ref. [9]
[b]Ref. [10]
[c]Ref. [11]

The derived expression for the threshold voltage in (5) was for the basic two layer structure without any coating layers. In practice, the phase-change layer is coated with a thin protective layer to prevent oxidation and for tribology purposes having finite electrical and thermal conductivity. To study the influence of the coating layer on the threshold voltage, Laplace's equation directly underneath the tip can be solved subject to the continuity of currents and voltages across the coating layer/phase-change layer interface yielding the modified threshold voltage:

$$V_t = \left(\frac{\sigma_t}{\sigma_{coat}} \delta_{coat} + \delta_p \right) \sqrt{\frac{k_t G (T_t - T_o)}{\sigma_t}} \tag{6}$$

where δ_{coat} and σ_{coat} are the thickness and electrical conductivity of the coating layer. The influence of the thermal conductivity of the coating layer k_{coat} is included in the factor G which is now modified to:

$$G = \frac{1}{k_p \delta_p} \left[\frac{H_t}{1 + H_t (\delta_{coat} / k_{coat})} + \frac{H_b}{1 + H_b (\delta_u / k_u)} \right] \tag{7}$$

where H_t now refers to the thermal coefficient at the top of the coating layer. Equation (6) is plotted in Fig. 3 for a 2 nm coating layer with electrical conductivity of 50 $(\Omega m)^{-1}$ (a value laying between the electrical conductivities of the amorphous and crystalline phases to avoid current shunting [4]). The top surface of the coating layer is assumed to be thermally insulated with $H_t \rightarrow 0$. Fig. 3 shows that the threshold voltage is now large at small thickness, has a minimum around 13 nm, and reaches the no coating limit for large phase-change layer thicknesses. Hence the introduction of a coating layer alters the square root dependence of the threshold voltage on phase-change layer thickness and this behaviour is controlled by the thickness, thermal and electrical conductivity of the coating layer.

4. CRYSTALLINE DOT DIAMETER

The approximate diameter of a recorded crystalline mark may be determined from the transition temperature isotherm. For applied voltages that are equal to or greater than the threshold voltage, the location of the transition temperature isotherm can be determined by substituting the electric field in (4) for the region $x > L/2$ into (3) and solving for x at $T = T_t$; this yields:

$$x_o = \frac{L}{2} + \frac{d}{2\delta_p}\left\{\sqrt{\frac{P}{k_t G(T_t - T_o)}} - 1\right\} \tag{8}$$

This shows that the location of the transition temperature isotherm (and hence the diameter of a recorded mark) depends on the tip contact length, the power supplied, and thicknesses and thermal properties of the phase-change and adjacent layers. At the threshold voltage, the power density is $P_t = k_t G(T_t - T_o)$ and the transition temperature isotherm is at the corner of the tip (i.e. $x_o = L/2$) thus defining the minimum crystalline dot size. At voltages a factor F larger than the threshold voltage, the transition temperature isotherm is thus given by:

$$x_o = \frac{L}{2} + \frac{d}{2\delta_p}(F - 1) \tag{9}$$

The diameter of the recorded crystalline dots (assuming circular dot shapes) is therefore $2x_o$. The power supplied for crystallisation can therefore be written for a cylindrical depth profile of the dot as:

$$P_s = F^2 k_t G(T_t - T_o)\pi x_o^2 \delta_p \tag{10}$$

Equations (9) and (10) are plotted in Fig. 4 as functions of the phase-change layer thickness and are compared with published experimental values in ref. [3]. In this figure, the applied voltage was 1.2 times the threshold value with an assumed tip contact length of 20 nm. The remaining parameters are the same as for the other figures. The calculated dot diameters in Fig. 4 are equal to the tip contact length at small medium thicknesses, and increase with increasing medium thickness in line with the experimental measurements. The discrepancy between the measured and calculated dot diameters is due to the fact that the authors in ref. [3] used two different types of tips in their experiment with two different contact lengths while in Fig. 4 only one contact length was used. Moreover, the voltages in ref. [3] were applied through a series resistor causing the voltage drop across the phase-change layer to vary with change in conductivity and hence its value is uncertain, while the calculations in Fig. 4 assumed a fixed applied voltage.

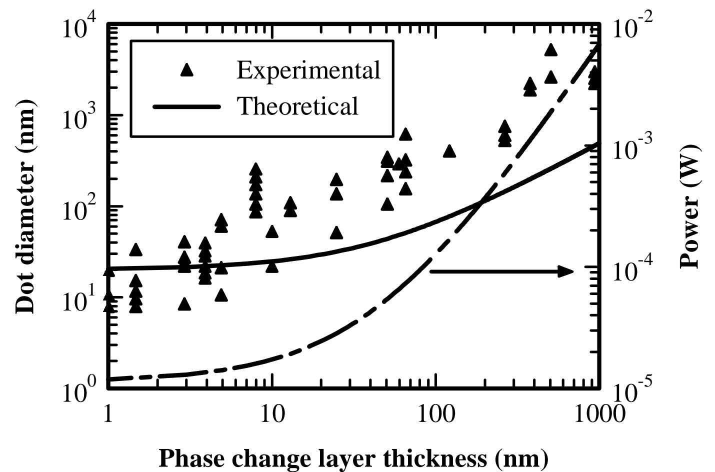

Fig. 4 Calculated crystalline dot diameters and power of crystallisation compared with measurements from ref. [3].

4. TRANSITION LENGTHS

The linear and areal densities of probe storage systems is determined according to how close bits can be written together before they start to overlap. This is mainly determined by the size and depth profile of the recorded bit [5, 6], and also by the extent of the amorphous to crystalline transition region. The size and shape of recorded bits is

influenced by the profile of the heat source, the dimensions, the electrical and thermal properties of the adjacent layers, and the electronic and kinetic processes occurring during the recording operation [5, 6]. To this effect a simplified analytical theory, based on the slope approach, was developed that illustrate how these processes conspire to influence the extent of the amorphous-to-crystalline region [12].

The slope theory, having its origins in magnetic recording, solves the slope equation:

$$\frac{\partial \sigma_p}{\partial x} = \frac{\partial \sigma_p}{\partial T} \times \frac{\partial T}{\partial x} \tag{11}$$

at one spatial location for a transition length parameter that relates to the extent of the amorphous-to-crystalline transition. The location at which the slope equation is solved is the location of the transition temperature isotherm as determined from (9). Each term of the slope equation will be determined next.

The first term in (11) is the spatial gradient of the conductivity transition which is assumed to follow the exponential profile [12]:

$$\sigma_p = \begin{cases} \sigma_t \exp[-(x - x_o)/a], & x \geq x_o \\ \sigma_c - (\sigma_c - \sigma_t)\exp\left[\dfrac{\sigma_t (x - x_o)}{a(\sigma_c - \sigma_t)}\right], & x < x_o \end{cases} \tag{12}$$

where σ_c is the electrical conductivity of the crystalline phase and is taken to be much larger than the amorphous phase, and a is the transition length parameter. The slope of the conductivity profile at the transition temperature is:

$$\left.\frac{\partial \sigma_p}{\partial x}\right|_{x_o} = \frac{-\sigma_t}{a} \tag{13}$$

where the transition length parameter a determines the extent of the transition region given by $a\sigma_c/\sigma_t$.

In the presence of this conductivity profile, the resulting temperature distribution in the phase-change layer can be evaluated by substituting (12) and the electric field from (4) into the heat equation for this system in (1) and solving subject to the appropriate boundary conditions described in [12]. The spatial gradient of this temperature evaluated at the transition position given in (9) may be approximated by [12]:

$$\left.\frac{\partial T}{\partial x}\right|_{x_o} \approx -\sqrt{G}(T_t - T_o)\left\{\frac{1}{1 + a\sqrt{G}}\right\} \tag{14}$$

where equation (14) implies that the gradient of the temperature at the transition temperature isotherm has little sensitivity to applied voltages greater than the threshold value for small phase-change layer thicknesses.

The variation of electrical conductivity with temperature is related to the crystallisation kinetics and change of electrical conductivity with crystallisation fraction χ, and hence can be expressed as:

$$\frac{\partial \sigma_p}{\partial T} = \frac{\partial \sigma_p}{\partial \chi} \times \frac{\partial \chi}{\partial T} \tag{15}$$

The variation of crystalline fraction with temperature can be determined from Johnson-Mehl-Avrami-Kolmogorov (JMAK) model using a linear heating regime with constant heating rate, and taking that the transition temperature occurs at the peak crystallisation rate [12]. For small heating rates (up to ~ 10 K/min), the gradient of crystalline fraction with temperature was found to be:

$$\left.\frac{\partial \chi}{\partial T}\right|_{T_t} = \frac{E_c}{eRT_t^2} \tag{16}$$

where E_c is the activation energy of crystallisation, $e = 2.7183$, and R is the Boltzmann constant. At very high heating rates, (16) is multiplied by the Avrami exponent n [12]. To relate the electrical conductivity to crystalline fraction, a generalised form of Bruggeman's mean field formula can be used [13], and when the crystalline conductivity is large compared to the amorphous conductivity:

$$\sigma_p = \sigma_c \left(\frac{\chi - \chi_c}{1 - \chi_c} \right)^r, \qquad \chi_c \leq \chi \leq 1 \tag{17}$$

where χ_c is the critical volume fraction or percolation threshold, and r is an exponent determining the extent of change of electrical conductivity with crystalline fraction. Differentating (17) with respect to χ and evaluating at the transition temperature where $\chi = \chi_t \approx 0.6321$ yields:

$$\left.\frac{\partial \sigma_p}{\partial \chi}\right|_{T_t} = \frac{r\sigma_t}{\chi_t - \chi_c} \tag{18}$$

Substituting (13), (14), (16) and (18) into the slope equation (11) and solving for the transition length parameter yields:

$$a = \frac{1/\sqrt{G}}{\left(\frac{r(T_t - T_o)}{\chi_t - \chi_c} \right) \left(\frac{E_c}{eRT_t^2} \right) - 1} \tag{19}$$

The transition length can therefore be reduced (increased linear density) by reducing the thermal characteristic length $1/\sqrt{G}$, and increasing the ratio of activation energy to transition temperature. A small thermal characteristic length can be achieved by reducing the thickness of the phase-change layer, and by enhancing heat produced in the phase-change layer to dissipate vertically through the adjacent layer to allow the temperature profile to follow the supplied power density profile thus increasing the temperature gradient at the transition location. This is shown in Fig. 5 where the transition length is plotted as a function of the dimensionless ratio $E_c(T_t - T_o)/RT_t^2$ for three different recording layer thicknesses. Also shown on this figure are the transition lengths for three phase-change compositions that are widely used in data storage applications.

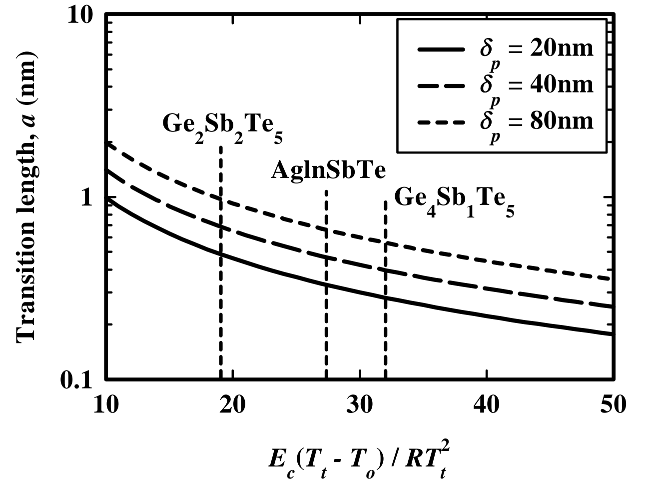

Fig. 5 Calculated transition lengths for different phase-change layer thicknesses. Calculation parameters: δ_u=20nm, L=20nm, k_p=0.4W/mK, k_u=50W/mK, H_t=0W/m^{2}K, H_b=2×10^{8}W/m^{2}K, χ_c=0.15 and r=1.

5. CONCLUSION

A simplified analytical theory was produced that relates the writing voltage and expected mark sizes in electrical probe storage systems on phase-change media to prominent system parameters such as the recording and adjacent layers thicknesses and thermal and electrical properties, tip contact length, and kinetic parameters of the recording

layer. An expression for the threshold voltage was derived showing a square root dependence on phase-change layer thickness in agreement with published measurements, but this dependence changes when introducing a coating layer. Theory in this work also showed that dot sizes scale with the tip contact length and increase with increasing recording layer thickness. A slope theory approach was utilised to predict the extent of the amorphous-to-crystalline region which provides information on how close marks can be written next to each other before they start to overlap. This theory showed that the transition length can be reduced by allowing heat to flow vertically through the sandwiching layers making the temperature distribution in the phase-change layer follow closely the more localised electric field produced by the tip/underlayer arrangement. Reducing the medium thickness also reduces the transition length.

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Biographies

Mustafa M Aziz recieved the B.Eng. degree from the University of Salford, Salford, U.K., in 1995, and the Ph.D. degree from the University of Manchester, Manchester, U.K., in 1999, both in electronic engineering. His doctoral research, and subsequent time as a research fellow at the University of Manchester, focused on theoretical modeling and experimental measurements of the write, read, and noise processes in thin-film and particulate magnetic storage media. He joined the School of Engineering, Computer Science and Mathematics, University of Exeter, Exeter, U.K., in 2001, as a lecturer in electronics, where he has now extended his research interests to the modeling of electrical probe storage on phase-change media.

C. David Wright was born in Thornaby-onTees, U.K., in 1957. He received the B.Sc. degree in physics from the Imperial College of Science and Technology, London, U.K., in 1978, the M.Sc. degree in solid-state physics from the University of Sheffield, Sheffield, U.K., in 1980, and the Ph.D. degree in perpendicular magnetic recording from Manchester Polytechnic, Manchester, U.K., in 1985. He took up the Chair in Electronic and Computer Engineering in the School of Engineering, Computer Science and Mathematics, University of Exeter, Exeter, U.K., in 1999. Prior to that, he was a Reader in Data Storage with the Department of Computer Science, University of Manchester, Manchester, U.K. His main area of expertise is experimental and theoretical characterization of the recording and readout processes in optical, magnetic, solid-state, and probe based memory systems and devices. He leads the U.K. Government (DTI)-funded "UK Data Storage Network" that aims to initiate and enhance U.K. industrial-academic cooperation in data storage research. He has been a partner in numerous European Union-and U.K.-funded research projects investigating new forms of probe, optical, and solid-state memories and has collaborated at some time or other with most of the major data storage companies in Europe, including Philips, Thomson, MPO, Plasmon, and GEC-Plessey.