# Recent Progress of Phase Change Random Access Memory (PRAM)

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**ABSTRACT**

Phase-change random access memory (PRAM) is one of the best candidates for high scale non-volatile memories due to its high programming speed, excellent endurance, and compatibility with unidirectional diode operation. However, D0 and D1 states in PRAM are produced by heat, which can induce the thermal disturbance between adjacent bits as the cell arrays continuously shrinks. Therefore, the shape of PRAM cell is changing from the conventional planar type with patterning process into the GST confined type cell, in which the reset current can be reduced dramatically and the interfaces between the cells block the heat propagation into the adjacent cell effectively. In recent, GST is confined to narrower ring type trench in order to attain much smaller reset current.

PRAM has a large resistance difference between set and reset states, so the research to introduce additional 2 data states between D0 and D1 has been carried out. In order to achieve the stable 4 level multi level cell (MLC) operation and avoid overlap of two adjacent resistance level, resistance drift of amorphous phase has to be minimized. Drift is known as coming from structural distortion when melt-quenched into amorphous and its relaxation with time, so the reduction of the distortion can be the way to minimize drift of amorphous resistance and achieve the stable MLC operation. The additional 2 data states have to be written by programming algorithm because the programming windows of the additional 2 states are smaller than the D0 and D1. As reported about various write and verify algorithms, we tested falling time variation as well as amplitude variation of programming pulse. In this paper, we review the progress of cell array scaling and state of the art of MLC in PRAM, and estimate the write and verify algorithm.

**Key words**: confined GST, reset current, write verify, multi level cell (MLC)

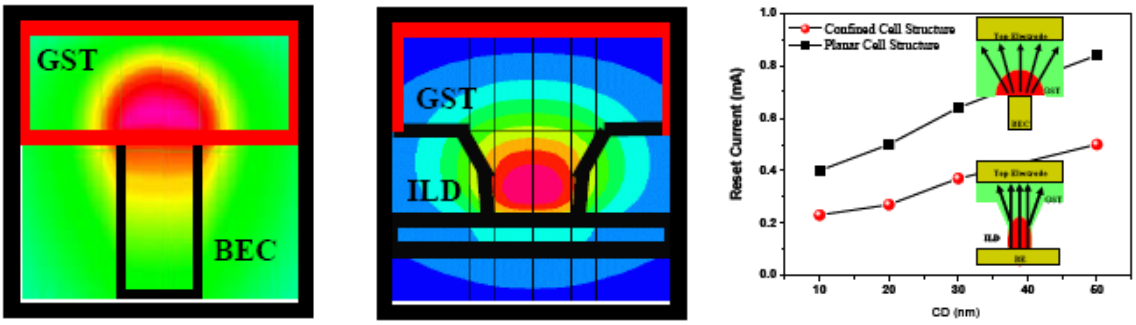
## 1. INTRODUCTION

Flash memories have been scaled down continuously since its introduction and become the mainstream of non-volatile memory (NVM) technology. In recent, phase-change random access memory (PRAM) has been attracting a considerable interest in view of the increasing scaling difficulties of NAND and NOR Flash memories. Since the early discovery of Stanford Ovshinsky in 1968 [1], improvements in phase-change material technology paved the way for development of commercially available compact disk rewriteable (CD-RW) and digital versatile disk (DVD) [2-5]. These advances, coupled with significant technology scaling and better understanding of fundamental physics of device operation, have motivated development of the PRAM technology at the present technology node [6]. However, high reset current, heat disturbance, and etch damage at the conventional planar type cell should be overcome in order to be more scaled. Many kinds of confined type cell which have been ever reported can be the solution of these problems [7,8].

PRAM has a wide range of resistance, and shows a large resistance difference between set and reset states. Therefore, additional 2 states can be added between them, and we can embody 4 level (2bit) multi level cell (MLC) PRAM. However, the time dependent resistance increase, so-called drift, can induce the overlap between adjacent 2 states in 4 level MLC, and the programming window of the additional 2 states is rather narrow. Therefore, the programming algorithm should be able to program and verify each 4 level of the resistance in a fine step.
In this work, we investigated a various type of etchless confined cell in which GeSbTe (GST) is confined into a few tens of nanometer sized trench, and studied the programming method for additional 2 states in 4 level MLC PRAM and resistance drift.

## 2. EXPERIMENTS

The planar type has been employed as the structure of GST cell since the introduction of PRAM as shown in Fig 1 (a). In this structure, heat generated right above the interface between GST and bottom electrode contact (BEC) can be dissipated in all directions. In order to reach above the melting temperature of GST, a large amount of heat and current should be needed in this structure due to the isotropic heat dissipation. In addition, the etch damage can be the fatal problem with progress of shrink. As the cell size shrinks, the spacing between programmed hemisphere and side wall of GST cell becomes shorter. In short spacing, the etch chemistry remained at the side wall can affect the programmed hemisphere, thereby changing the electrical properties of GST. In the line type GST in which each cell in the direction of bit line is not isolated, but shares the same GST line, each cell in the same bit line can suffer from the heat disturbance from the adjacent cell under programming operation. In order to avoid these problems, new type cell should be employed. As mentioned in the previous paper [7-8], confined structure in which the trench of a few tens of nanometer is filled with GST can be the best candidate of next generation cell type, as shown in Fig 1 (b). In this work, we use the chemical vapor deposition (CVD) process to fill the trench with GST, followed by the chemical mechanical polishing (CMP) process to flatten the surface of GST.




(a) (b) (c)

Fig. 1 (a) Cross sectional figure of conventional planar type cell and simulated results of heat generation
(b) Cross sectional figure of pillar type confined cell and simulated results of heat generation
(c) Scaling trends of cell size and reset current for both planar type and confined type cell

## 3. RESULTS & DISCUSSION

In this confined structure, heat dissipation can be minimized due to the interception of the lateral dissipation, which can leads to the reduction of reset current (current to make amorphous), as shown in Fig. 1 (c). The effect that the programmed volume would be influenced from the etch chemistry can also be reduced because the programmed volume is isolated into the trench. Because of undamaged cell from etchless process, the dispersion of the set and reset resistances can be minimized and the distribution of data can be improved. By the isolation of heat from the adjacent cell, the heat disturbance was dramatically reduced rather than that of conventional planar type.

The final shape of the GST confined type cell is shown in Fig. 2. The BEC material and interlayer dielectric (ILD) are flattened by CMP, and BEC material is removed to the middle point of the total height by etch back process. Then, the trench is filled with GST, and the rugged surface of GST is polished flat. As GST is stacked vertically above BEC in the cylindrical trench, the reset current is reduced due to the minimal heat dissipation into the lateral direction. According to Fig. 3, the planar and confined type cell make a distinct difference in reset current. The reset current of the confined type cell represents about one third of that of planar type. In order to more reduce the reset current than that of this confined type cell, the size and type of trench should be changed. Ring type BEC that has been already reported [9], as shown in Fig. 4 (b), can be used to fill both of the BEC and GST vertically, in which BEC material is filled and subsequently recessed to the middle point of the total height by etch back process, and then GST is deposited by CVD process followed by CMP process. In this structure of Fig. 4 (c), GST is formed in the same shape of the BEC, thereby melting and quenching in the shape of ring. Because only a partial thickness of GST in ring shape participates in melting, and the lateral heat dissipation is interrupted, reset current can be reduced considerably compared with the pillar type confined cell of Fig. 2. Fig. 5 (a) reveals the vertical SEM image of the as-trenched state of ring type confined cell after the BEC material is removed to the half point of the height. Fig. 5 (b) shows the vertical SEM image before GST is filled in the trench, and Fig. 5 (c) is the cross sectional TEM image after the ring type confined cell is completed. The chemical analysis of the GST composition is also represented, which is in good agreement with the expected value. When programming reset state, the amorphous volume is considered to be reached from the interface with BEC to the middle point of the GST height.

The difference between set and reset resistances in PRAM is so large that additional 2 states can be added between set and reset states, which can enable 4 level multi level cell (MLC). As speculated from Fig. 3, voltage range of programming additional 2 states is too small to program at a time, so it needs for ‘write and verify’ (WAV) to be employed. If programmed results does not fall within the range of targeted level, amplitude of programming voltage is increased or decreased by a predefined step, as depicted in Fig. 6 (a). The distribution of programmed 4 level resistances by this WAV is presented in Fig. 6 (b), in which the resistance drift 1 day after programming is also shown. It is seen that there is a sufficient sensing window between each levels. It is important to the reliability of MLC operation whether the resistance drift can saturate. Because the drift at high temperature is known to be higher than that at room temperature, it is tested at 85’C and 100’C for 10hr whether there will be the drift saturation, as shown in Fig. 7. There is no difference in drift coefficients between 85’C and 100’C, but the drift progresses continuously without saturation after both of the annealing treatments. According to the structural relaxation (SR) model [10], it can be considered that there still remain some amount of defects in amorphous that play as a donor of electron to the conduction band.

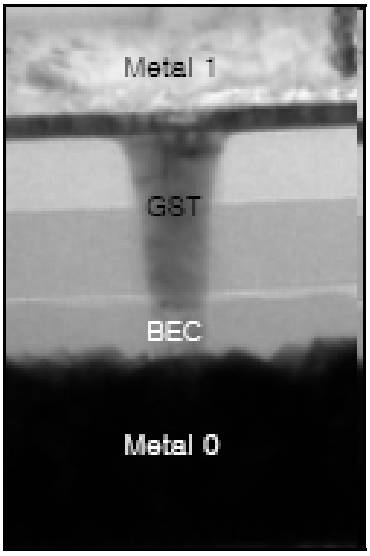



Fig. 2 Cross sectional TEM for pillar type confined cell

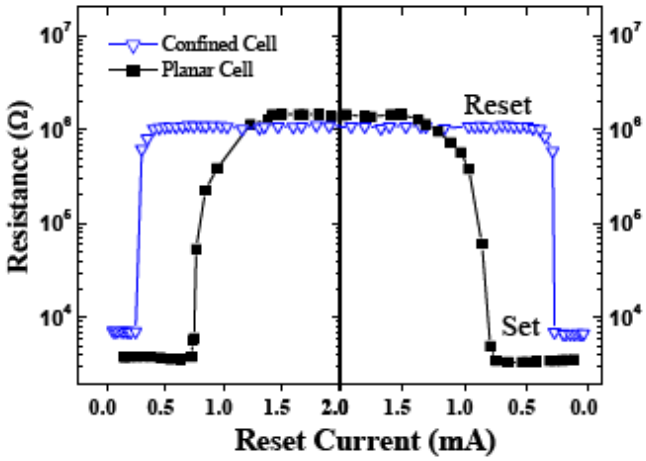
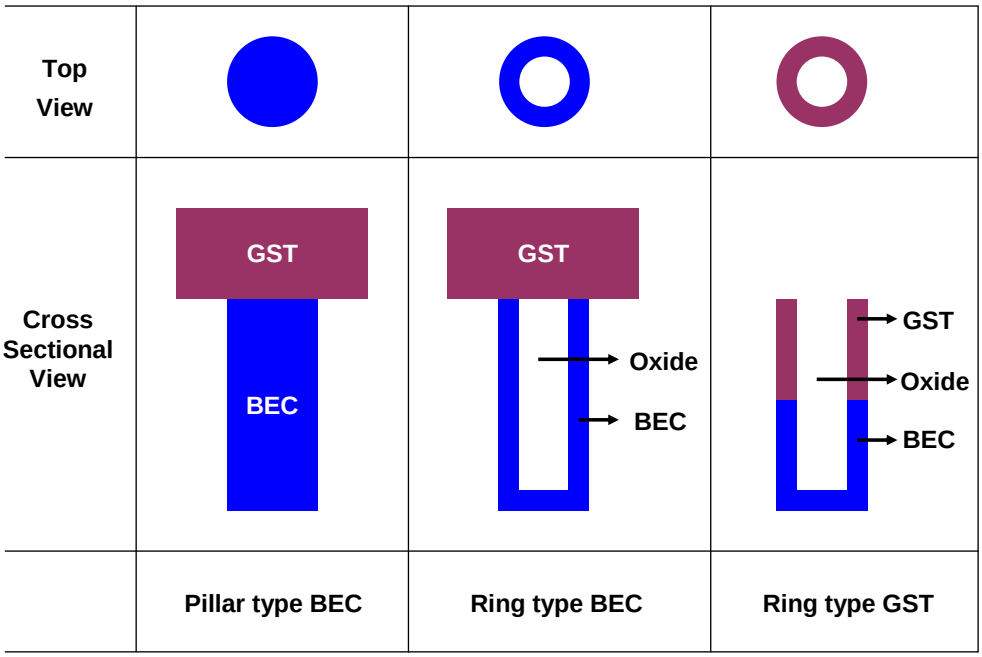
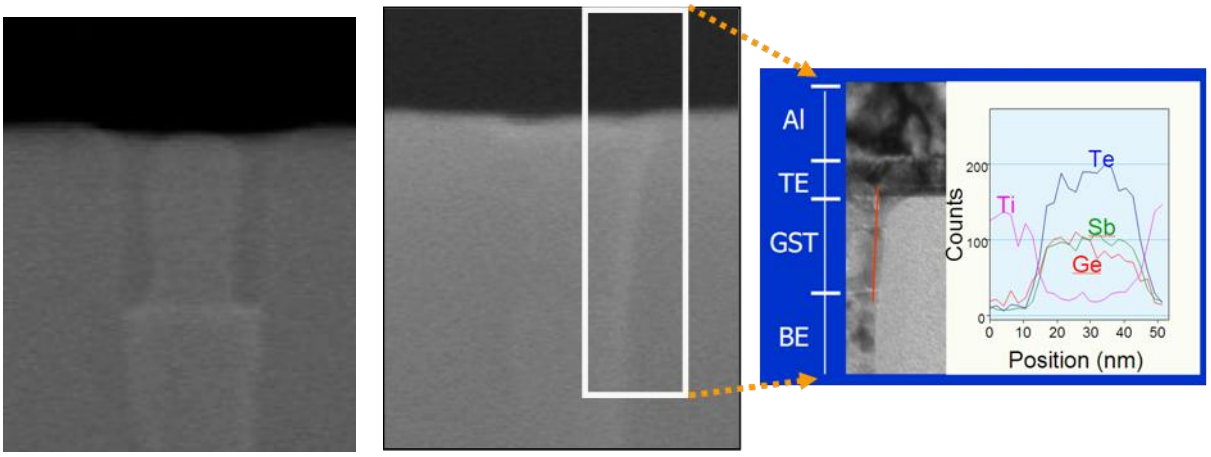



Fig. 3 Comparison of reset currents of planar type cell and pillar type confined cell



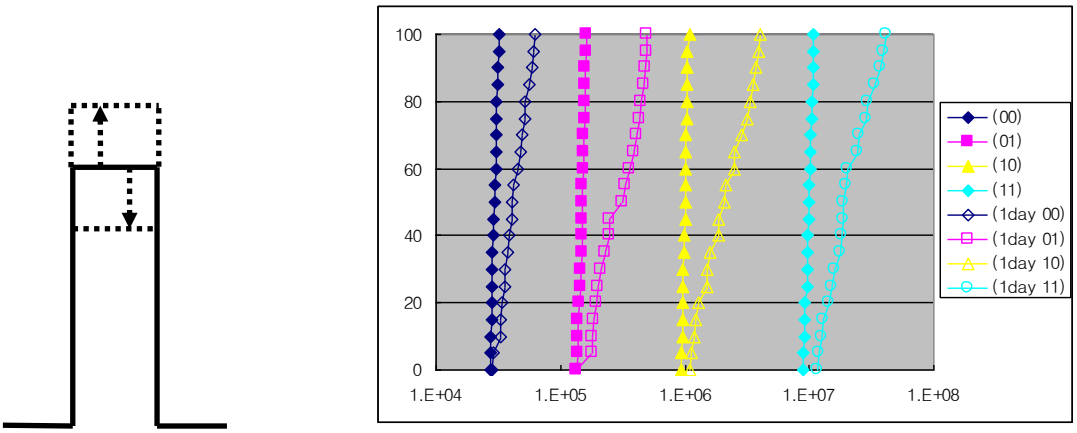

(a) (b) (c)

Fig. 4 Schematic diagram of (a) pillar and (b) ring type BEC, and (c) ring type confined cell




(a) (b) (c)

Fig. 5 (a) Vertical SEM image of as-trenched state of ring type confined cell
(b) Enlarged vertical SEM image before GST is filled in the trench
(c) Cross sectional TEM image of ring type confined cell and its chemical analysis




(a) (b)

Fig. 6 (a) Pulse shape and voltage step used in write and verify (WAV) method
(b) Distribution of 4 level resistance programmed by WAV and its drift results

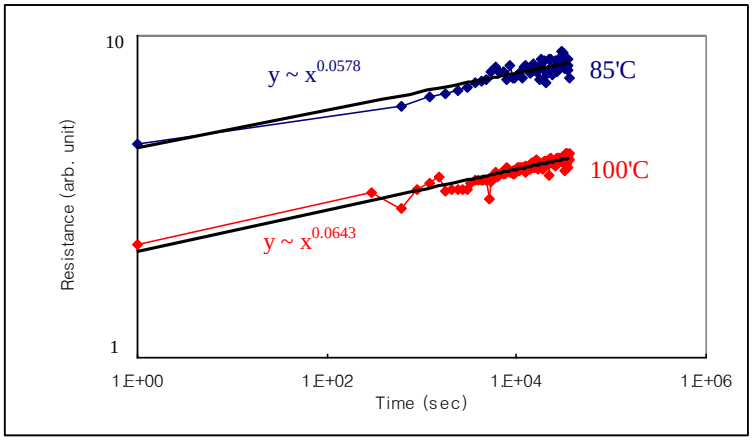



Fig. 7 Resistance drift after annealing at 85’C and 100’C to confirm whether there will be drift saturation

## 4. CONCLUSION

As the cell size shrinks, heat disturbance between adjacent cells is the important problem. Therefore, GST confined type cell was introduced. The pillar type confined cell shows the reduction of reset current and superior heat blocking between adjacent cells rather than planar type. The trial to more shrink the cell size leads to the ring type confined cell which reveals the lower reset current than that of pillar type confined cell.

Additional 2 states can be programmed between the set and reset states due to the large difference between them. Voltage amplitude modifying WAV was tried to program the additional 2 states, which are well distributed without dispersion by WAV.

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