Progress and Perspective of Phase-Change Memory

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ABSTRACT

Phase-Change Memory (PCM) has been introduced in the Non-Volatile Memory (NVM) arena as the most promising candidate to replace existing technology, e.g. Flash memory. The fantastic scaling capability of the Flash technology has delayed the introduction in the market of the PCM technology, although the progresses so-far have been all positive, in terms of cell size, process complexity, performances, reliability. The technology is able to provide high density product demonstrators at 90nm, with cell size in the order of $8F^2$ and unique specification. In particular we propose original µTrench-based cell architecture for PCM, with low-programming current and good dimensional control of the sub-lithographic features, which allow us to extend the technology to scaled node. In fact one of the key points for the future road-map of NVM is the scalability of the technology, either the established one or the emerging. PCM shows the capability to scale and it is possible to forecast cell architecture well beyond the 2x nm technology node.

Key words: memory, non-volatile, phase-change, chalcogenide, scaling

1. INTRODUCTION

Flash memories have been able to scale for more than 15 years, boosting the recent impressive growth of the portable equipment market and becoming the mainstream NVM technology. Projecting into the next decade, though, there are several fundamental limitations that must be solved to push the floating-gate concept beyond the 32nm technology node. The increasing complexity of floating gate scaling leaves room for the investigation of alternative NVM concepts that promise better scalability, improved performances, and competitive cost with Flash. PCM is one of the most promising candidates for next-generation NVM, having the potentiality to improve the performance compared to Flash - random access time, fast read throughput, write throughput, direct write, bit granularity, endurance - as well as to be scalable in the deca-nanometer range [1].

Despite the high potential of the PCM concept and the good integration results so far achieved [2,3], some practical challenges must still be addressed. In particular, large efforts are being dedicated to the integration of a compact PCM cell structure with the chalcogenide compound, to achieve a full compatibility with an advanced CMOS technology and to reduce the programming current without degrading the appealing features of the PCM technology. Several approaches have been so far proposed to achieve low reset currents [4-7], none of them being completely satisfactory from the point of view of sustainable process complexity and controllable program current. The so called lateral cell approach has demonstrated currents as low as 200 µA [4], but its integration in multi-megabit arrays has not yet been proven. Nitrogen doping [5] is another effective technique to reduce the programming current, but with the drawback to largely increase the set resistance, thus degrading the capability for a fast random read out of the cell status. The in-line memory cell [6,7] with the self-heating concept promises enhanced performance in terms of programming currents (less than 100 µA), but the reported results are not well understood and its potentiality at this stage cannot be clearly assessed. The so called Lance architecture [2,5], with its compact and vertical integration, requires larger programming currents and gives larger spreads if compared with µTrench using the technological constraints [2]: it could become viable only when modified into the Ring-type heater [8], with additional process complexities which require dielectrics with very good gap-filling properties and compatibility with heater material.

Among these alternatives, the µTrench PCM cell architecture represents a well-tempered fusion of all the appealing features of the PCM technology, having been demonstrated to simultaneously achieve low programming currents, small cell size, good dimensional control, and proven multi-megabit manufacturability [2,9]. Moreover, the fine tuning capabilities of the PCM µTrench cell and its potentialities to obtain very low programming currents have been largely demonstrated, with an optimized µTrench cell that achieved a programming current of 400 µA at 90nm [2].

Aim of this work is to discuss the current status of Phase-Change Memory, moving from the electrical results obtained with the µTrench architecture and highlighting its strength in view of the continuous scaling of semiconductor technology, eventually down to the 2x nm node.

2. EXPERIMENTS

Since 2001 we have been developing an original and innovative architecture for Phase-Change Memory, called μTrench. The new key concept introduced in this architecture, that keeps the programming current low and maintains a compact vertical integration, is the definition of the contact area between the heater and the GST by the intersection of a thin vertical semi-metallic heater and a trench (that we call "μTrench"), in which the GST is deposited. The resulting structure is schematically depicted in Fig.1. Since the μTrench can be defined by sub-litho techniques and the heater thickness by film deposition, the cell performance can be optimized by tuning the resulting contact area, today around 1000 nm^2, still maintaining a good dimensional control.

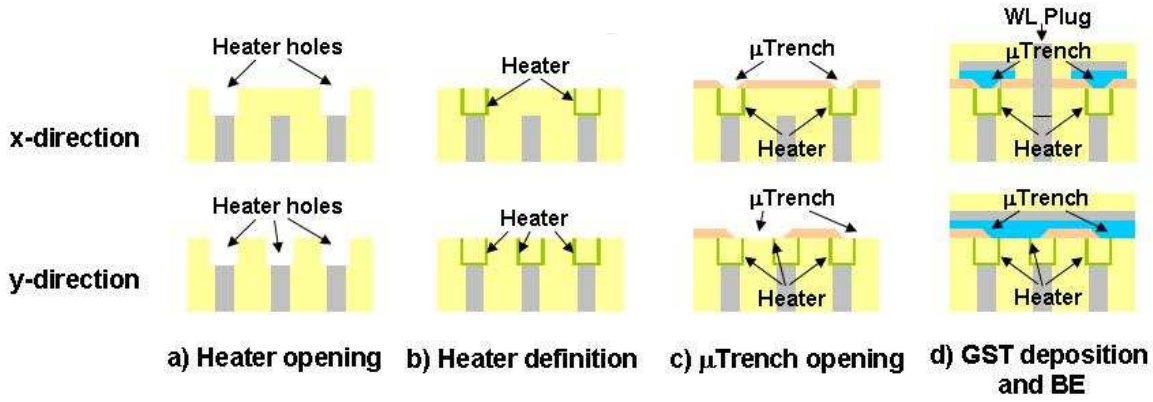

Fig.1. Schematic description of μTrench fabrication steps

A vertical PCM cell employing the $Ge_2Sb_2Te_5$ (GST) chalcogenide alloy has been integrated into an advanced 90nm CMOS technology (Tab.1). The PCM cell is integrated adding the basic process modules, i.e., heater and GST, between the FEOL and BEOL blocks (Tab.2). The PCM storage element is constituted by a variable resistance (heater and GST) and it needs a selector device in order to be addressed inside a regular array. As a selector we have chosen a common-collector *pnp* bipolar junction transistor, which allows a fully vertical integration of the cell and gives the small cell size required in high-density NVM. The resulting layout of the device is extremely compact with a cell area of 0.096 μm^2 and it is basically limited by the selector design rules. It is worth noting that this PCM architecture is also fully compatible with the use of a MOSFET selector, but in this case the resulting cell size is larger (20-40F^2): nevertheless it can be easily integrated with a minimum overhead of masks, thus being suitable for embedded NVM applications.

Lithography	**90nm**
Unit Cell Size	**0.22 x 0.44 μm^2**
Isolation	**270nm Shallow Trench**
Gate Oxide	**8 nm**
Gate Type	**Dual-flavour poly & $CoSi_2$**
Interconnects	**3 Cu**

Tab.1. CMOS technology basic parameters

Blocks	Modules
FEOL	STI
	Wells implantation
	MOSFET definition
	BJT formation
	Salicide formation
PCM formation	Pre-contact
	µTrench
	Metal0 (GST/cap)
BEOL	Contact/Via0
	Line1
	Via1/Line2
	Via2/Line3
	Pass & Alucap

Tab.2. Schematic process flow-chart

3. RESULTS & DISCUSSION

The scalability of the reset current has been experimentally assessed on different technology nodes with devices that demonstrated the manufacturability of large arrays [2,9]. The resulting values are reported in Fig.2, in which we reported also the forecasted currents for future scaled technology nodes, down to 22nm.

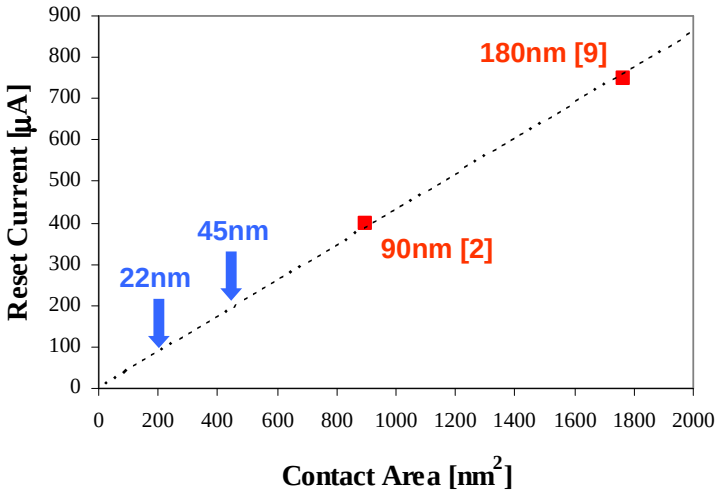

Fig.2. Measured (red) and projected (blue) scaling of reset currents for µTrench PCM technology

The reset current reduction shown in Fig.2 can be mainly ascribed to the increase of the heater thermal resistance, R_{TH}, with the diminishing of the contact area. As shown in Fig.3, the Joule heating mainly takes place inside the GST, where the voltage drop is constant and close to the holding voltage, (V_H in Fig.4 and in Fig.5).

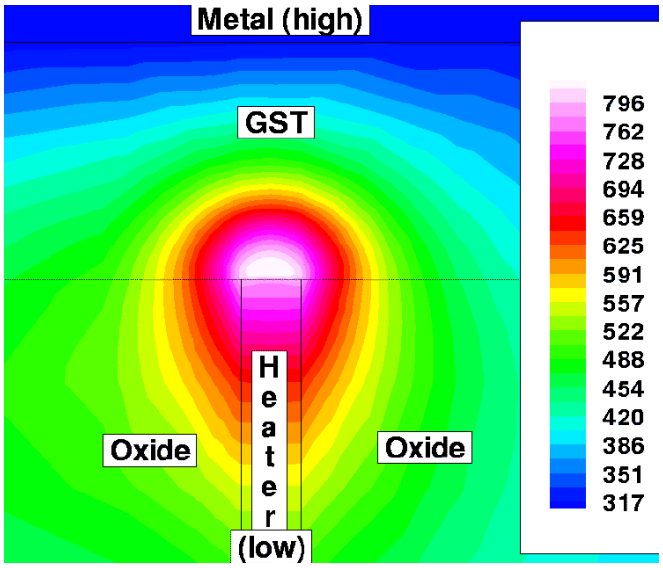

Fig.3. Simulation of temperature distribution during PCM programming

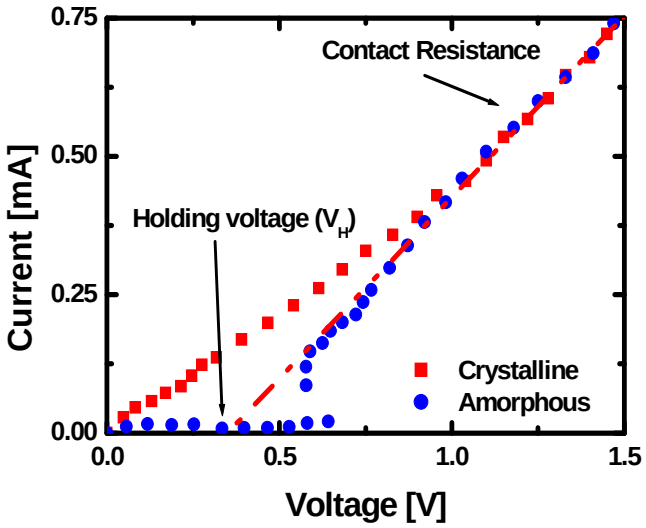

Fig.4. Schematic I-V characteristic of a PCM storage element

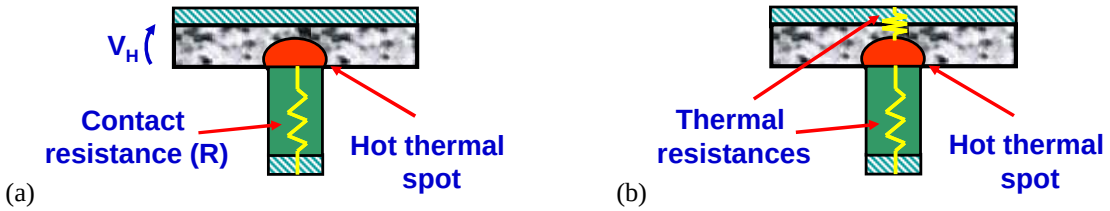

Fig.5. (a) Electrical and (b) thermal equivalent circuit of a PCM storage element

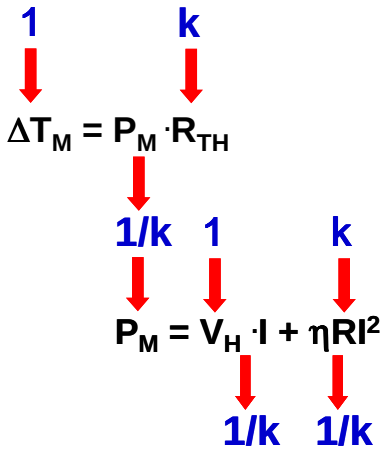

Fig.6. Basic laws for scaling of PCM programming current

Since the melting temperature is constant and R_{TH} increases, the power P_M required to melt the GST goes down. From the expression of the power injected into the thermal hot spot, it follows that a reduced current is required to reach the melting temperature. If the scaling is isotropic and the scaling factor is equal to $k > 1$, R_{TH} and R increase as k and programming currents decrease as $1/k$ (Fig.6). The previous argument holds true when a fixed geometry and thermal environment are considered: different cell architectures behave differently if compared at the same technology node.

One of the main concerns related to the PCM technology relies on the impact of the thermal cross-talk between adjacent bits. With the perspective to scale down the device dimension, the distance between cells in a high-density memory device is of the order of the minimum lithographic pitch. If a high current pulse is applied on one cell, the neighbor bits can reach the crystallization temperature, thus losing the stored information (Fig.7).

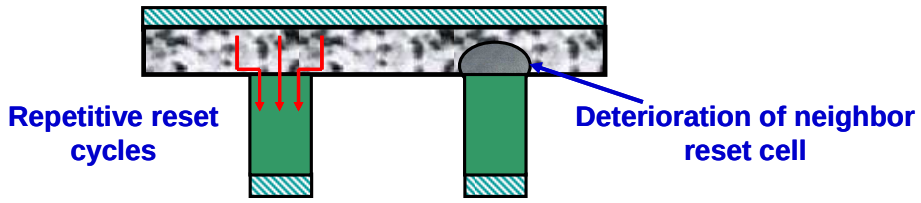

Fig.7. Schematic depiction of program disturb between adjacent bits

Fig.8 shows the crystallization time of amorphous cells as a function of temperature, demonstrating that 10 years data retention is guaranteed at temperatures lower than 110°C. Moreover the graph indicates that a cell can undergo 10^{10} reset pulses (each 100 ns long) without causing disturb to the adjacent bits if their temperature does not go above 195°C during these pulses.

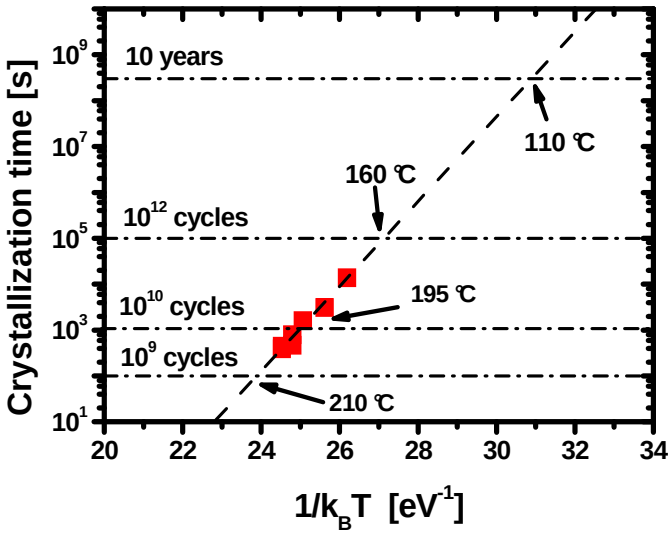

Fig.8. Data retention measured on µTrench PCM cell

On the other hand, Fig.9 shows the resistance of a typical cell in the amorphous state as a function of the program/erase cycles performed on an adjacent bit. Note that the high resistive state is not perturbed up to 10^9 cycles, which correspond to a thermal disturb lasting about 100 s for reset pulses of 100 ns. Fig.8 suggests that for a retention failure to occur after 100 s, the thermal disturb should heat the adjacent cell at 210°C. These results have been compared to numerical calculations [10] of the thermal crosstalk for a 180nm technology device. Fig.10 shows both transient and steady state (worst case) conditions. The 10 years line corresponds to the above 110°C limit. Considering 10^{12} cycles as target endurance, the corresponding 160°C limit is easily satisfied. The results confirm that thermal disturb is not a concern at 180nm node.

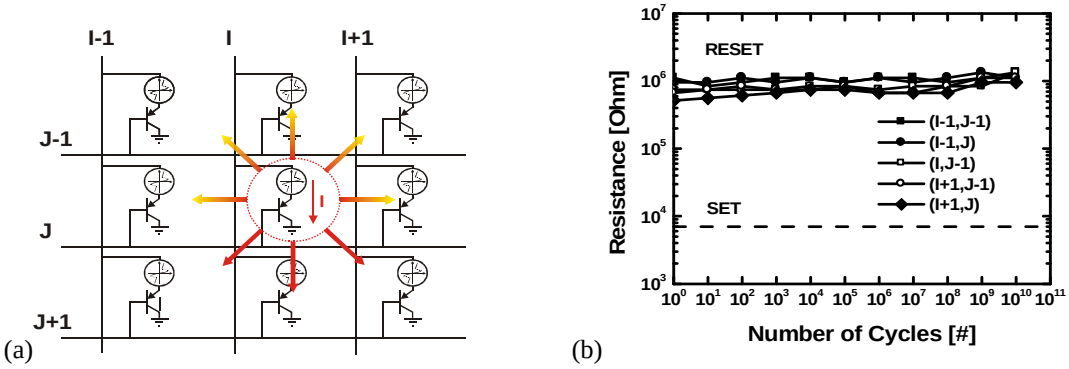

Fig.9. (a) Schematic depiction and (b) results of program disturb experiment on 180nm µTrench array

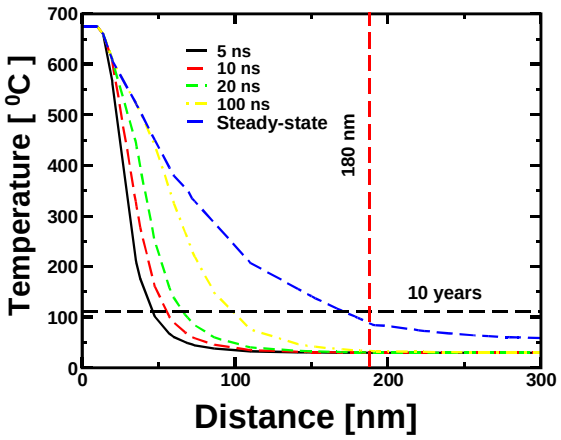

Fig.10. Thermal crosstalk simulation between adjacent bits at 180nm technology node

The same numerical model has been then used to investigate the scaling potential of PCM technology. Fig.11 shows the thermal cross-talk simulated for 65nm and 45nm technology obtained shrinking the 180 nm cell already analyzed in Fig.10 and without introducing optimized materials for the thermal insulation. Even in this worst case, the numerical results suggest a negligible thermal disturb between adjacent bits in both transient and steady-state condition. These results can be understood and extended to technology nodes beyond 45nm if we note that the heater is playing a dual role: when active it contributes to deliver power for melting and when inactive it constitutes a thermal boundary and it effectively cools its cell, preventing any possible disturb of the amorphous spot during programming of adjacent bits.

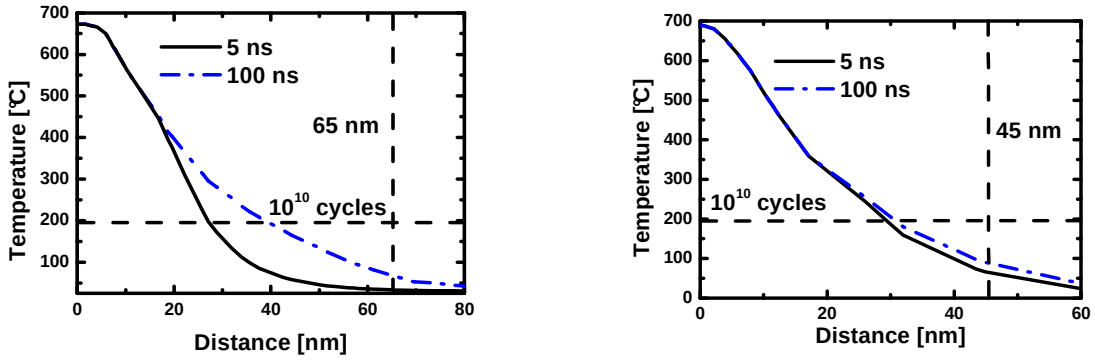

Fig.11. Thermal crosstalk simulations between adjacent bits at 65nm and 45nm technology nodes

Finally, it has to be noted that data retention of reset bits does not degrade with scaling [11], thus suggesting that amorphous spot is stable regardless of volume reduction. Moreover theoretical calculations [12] and experimental characterizations with conductive probe AFM [13] demonstrate that two stable phases can be toggled for sizes smaller than 10nm.

4. CONCLUSION

Phase-Change Memory is demonstrating a good level of maturity on 90nm technology node, both in terms of manufacturability and reliability. The achieved integration into standard CMOS platforms makes PCM an interesting technology to become eventually a mainstream in the Non-Volatile Memory market. Data collected at different technology nodes have shown a consistent scaling of PCM based on the μTrench architecture. Isotropic scaling allows linear reduction of programming currents and allows forecasting I_{RESET}~100uA at 22nm technology node. Data retention does not degrade when the contact area between chalcogenide and heater is reduced, thus highlighting another major strength of this memory. Finally, program disturb of adjacent cells is not an issue because of a self-compensating mechanism related to the dual role of the heater. All these evidences, together with an appealing cell size and some theoretical extrapolations confirm the high potentiality of Phase-Change Memory as an alternative technology for scaling down to 2x nm and beyond.

REFERENCES

[1] R. Bez and G. Atwood, “Chalcogenide Phase Change Memory: Scalable NVM for the Next Decade?”, NVSMW, pp. 12-15, 2006.
[2] F. Pellizzer et al., “A 90nm Phase-Change Memory Technology for Stand-Alone Non-Volatile Memory Applications”, Symp. on VLSI Tech., pp. 122-123, 2006.
[3] S. Kang et al., “A 0.1µm 1.8V 256Mb 66MHz Synchronous Burst PRAM”, ISSCC Tech. Dig., pp. 140-141, 2006.
[4] Y. H. Ha et al., “An edge contact type cell for phase change RAM featuring very low power consumption”, VLSI Symp. on Tech., 2003.
[5] S. J. Ahn et al., “Highly manufacturable high density phase change memory of 64Mb and beyond”, IEDM Tech. Dig., pp. 907-910, 2004.
[6] K. Elissa, F. Merget et al. “Novel lateral cell design for low current phase change RAM memories”, NVSMW 04, pp. 30-31, 2004.
[7] M. H. R. Lankhorst et al., “Low-cost and nanoscale non-volatile memory concept for future silicon chips”, Nature Materials, pp. 1-6, 13 March 2005.
[8] J.H. Oh et al., “Full Integration of Highly Manufacturable 512Mb PRAM based on 90nm Technology”, IEDM Tech. Dig., pp. 49-52, 2006.
[9] F. Pellizzer et al., “Novel µTrench Phase-Change Memory Cell for Embedded and Stand-Alone Non-Volatile Memory Applications.”, Symp. on VLSI Tech., pp. 18-19, 2004.
[10] A. Pirovano et al., “Scaling Analysis of Phase-Change Memory Technology”, IEDM Tech. Dig., pp. 699-702, 2003.
[11] R. Gleixner et al., “Data Retention Characterization of Phase-Change Memory Arrays”, IRPS, 2007.
[12] D. Wright et al., “Can We Reach Tbit/sq.in. Storage Densities With Phase-Change Media?”, EPCOS, 2004.
[13] T. Gotoh et al., “Minimal Phase-Change Marks Produced in Amorphous $Ge_2Sb_2Te_5$ Films”, J.J.Appl.Phys., vol. 43, no. 6B, pp. 818-821, 2004

BIOGRAPHIES

Roberto Bez was born in Milan (Italy) in 1961. He received the doctor degree in Physics at the University of Milan in 1985. In 1987 he joined the Central R&D department of STMicroelectronics and started to work on NVM technologies. In the 90s he has participated to the development the NOR Flash memory technology, in a first phase as expert of the device physics and reliability and in the second phase as project leader of the multilevel product development. In 2000 he started to investigate new NVM technologies, alternative to the floating-gate based Flash. Since 2001 he has been working on the development Phase Change Memory technology. Currently he is the high density and emerging memories director, in the NVM Technology Development of the Front-end Technology and Manufacturing group.

He has authored many papers, conference contributions and patents on topics related to NVM. He has been lecturer in Electron Device Physics at the University of Milan and in Non-Volatile Memory Devices at the University of Padova, Polytechnic of Milan and University of Udine.

Fabio Pellizzer was born in Follina (Italy) in 1971. He received the doctor degree in Electronic Engineering in 1996 from the University of Padova, Italy, with a thesis on characterization and reliability of thin gate oxides in MOS transistors. In 1998 he joined Central R&D department of STMicroelectronics in Agrate Brianza (Italy). Initially his work focused on thin dielectrics characterization and reliability for NVM technologies. Since 2002 he is in charge of process development for phase-change memories based on chalcogenide materials. He has authored many papers, conference contributions, and patents on phase-change memories.