Phase Change Alloys for Very High Temperature Data Retention Applicable for Automotive Applications

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ABSTRACT

Phase-change memory (PCM) alloys based on Germanium, Antimony and Tellurium (GST) with SiO_2 nanoscale dielectric inclusions are investigated for material and electrical properties. The addition of dielectric inclusions in select GeSbTe significantly increases the crystallization temperature and device data retention. In memory device configurations, the optimal nanocomposite alloys exhibit 10 year data retention above 200 ˚C, and a cycle life greater than $1x10^7$ cycles while maintaining set programming speed of 250 ns demonstrating PCM as an excellent candidate for both discrete and on-chip embedded memory in the demanding automotive microcontroller market.

Key words: Data retention, GeSbTe, GST, Nonvolatile memories, PCM, phase-change memory

1. INTRODUCTION

Key attributes of PCM as a future nonvolatile memory (NVM) solution are its inherent scalability, small cell size, improved cycle endurance over flash NVM, direct write (no erase), and high speed R/W performance. The most common PCM alloy, $Ge_2Sb_2Te_5$ (GST225), has an amorphous state that is stable for more than 10 years at an operating temperature of 100 ˚C or less. While the data retention temperature range of GST225 is sufficient for most consumer applications, it is too low for automotive applications requiring up to a 20 year lifetime at temperatures up to 175 ˚C. In addition, there are embedded memory applications where it is required to program at the wafer level and have the data remain intact through subsequent Pb-free solder reflow (260 ˚C for ~ 60 second).

Other groups have reported GST225 alloys reactively sputtered with N_2 or O_2 which resulted in a moderate increase in crystallization temperature on blanket films or data retention temperature in devices, however the improvement was insufficient to meet automotive level lifetime requirements or to retain data through a 260 ˚C Pb-free solder reflow. Addition of nanoscale dielectric inclusions in GST225 to provide programming current reduction has been reported previously by numerous authors, however, device data retention were not described. For a list of references on investigations of N_2, O_2 and nanoscale dielectric inclusions in PCM alloys, see the citations in Ref. [1],

2. EXPERIMENTS

The alloys and composites are based on GeSbTe (with variable compositions comprising GST225, GST415 and GST425), plus the addition of nanoscale SiO_2 dielectric inclusions by co-sputtering. Phase change memory devices were fabricated by co-sputtering 75 nm films at 100 °C in 2mT Ar using a pore type test structure [1]. Devices had 112 nm diameter bottom contacts and were characterized by pulsed current-voltage (I-V) measurements and measurements of programmed resistance versus programming current (R-I curves). Device cycling data was obtained by alternating SET and RESET programming pulses. Device SET speed was determined by measuring the resistance of an initially RESET device as a function of SET pulse width

3. RESULTS & DISCUSSION

The device data as shown in figures 1 & 2 indicate that the SET (crystalline) state resistance increases with increasing volume fraction of SiO_2 in GST415, however, there is less resistance increase for SiO_2 added to GST425. No strong dependence of either dynamic resistance during programming (dV/dI) or programming current is seen for these nanocomposites in contrast with earlier results observed when co-sputtering SiO_2 with GST225. In the GST225 case, both the dynamic resistance increased and programming current was lower with increasing SiO_2. Device SET speed

was determined by measuring the resistance of an initially RESET device versus SET pulse width. As shown in Fig.3 SET programming speed on 132 nm pore diameter devices measured ~250 ns for the 10% SiO_2 sample (~3X slower than GST415). Device cycling data was obtained by alternating 500 ns SET and 50 ns RESET programming pulses and stable device cycling in excess of $1x10^7$ cycles was observed up to 10% SiO_2 incorporation as shown in Fig. 4. The crystallization time, "time-to-fail" was obtained from curves like Fig. 5 using a demarcation level criterion (the geometric mean of the RESET and SET resistance at each temperature) and plotted versus 1/kT in an Arrhenius plot. In Fig 6 an Arrhenius plot of data retention shows extrapolated temperature for 10 year lifetime (based on first retention failure out of 24 devices). When SiO_2 nanoscale inclusions are added to GST225, data retention decreases, however, for GST415 and GST425, the addition of 10% SiO_2 increases the 10 year lifetime to above 200˚C.

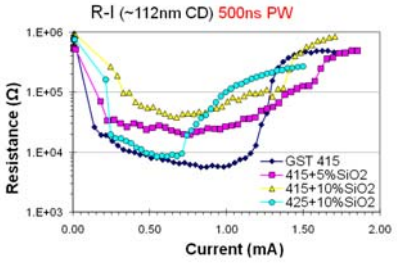

Fig. 1 Resistance vs. Programming Current

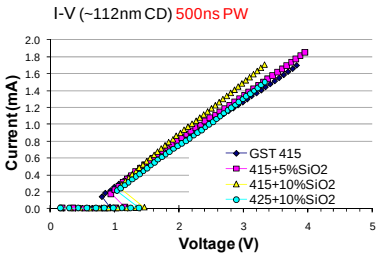

Fig. 2 Current Voltage characteristic curves

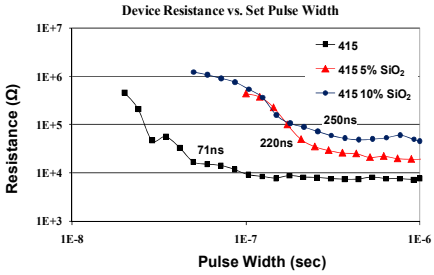

Fig. 3 Resistance versus SET pulse width after initial reset pulse

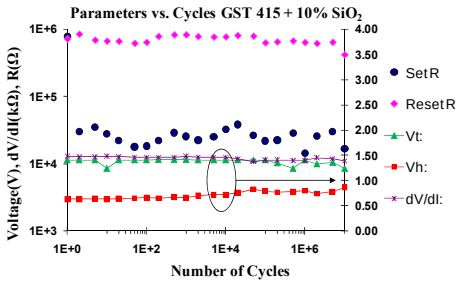

Fig. 4 Cycling endurance of SET and RESET resistance, threshold voltage, and holding voltage for GST415 + 10% SiO_2 device using sequential SET/RESET pulses

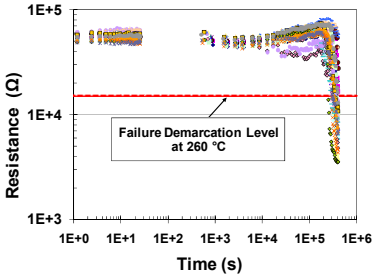

Fig. 5 Device resistance vs. time at 260 ˚C for 24 devices using GST415 + 10% SiO_2

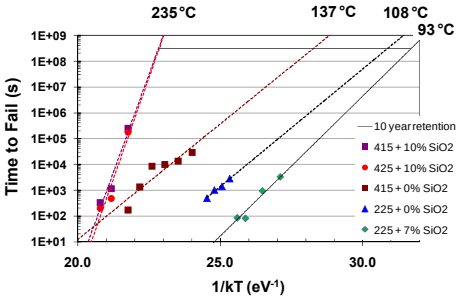

Fig. 6 Arrhenius plot of data retention showing extrapolated temperature for 10 year lifetime (based on first failure out of 24 devices

4. CONCLUSION

PCM devices using co-sputtered GST alloys with SiO_2 nanoscale inclusions were investigated and devices exhibited significantly different results depending on the GST composition. Adding SiO_2 to GST225 provides no improvement in data retention, however for GST415 and GST425 adding nanoscale SiO_2 inclusions significantly increases the 10 year device data retention to well over 200 ˚C and provides robust margin for surviving Pb-free solder reflow with data intact enabling PCM as a highly scalable non-volatile memory solution for most demanding automotive applications.

REFERENCES

[1] W. Czubatyj, S. Hudgens, C. Dennison, C. Schell, T. Lowrey, "Nanocomposite Phase Change Memory Alloys for Very High Temperature Data Retention" IEEE Electron Device Letters (accepted for publication 16 May 2010)