DRIFT OF PROGRAMMED RESISTANCE IN ELECTRICAL PHASE CHANGE MEMORY DEVICES

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ABSTRACT

A detailed experimental study of drift in PCM devices at different temperatures and with different memory alloys is presented.
It was shown that: drift exponent is reduced with decreasing chalcogenide film thickness, drift is observed to saturate with time, drift exponent rises and time of drift saturation decreases with increasing temperature. In this paper we report for the first time drift for more conducting alloys, which have drift maxima at intermediate resistance.
Drift dependence on programmed resistance, i.e. dependence on *d* vs. Ro and position of maxima of *d* vs. Ro. and *d* absolute value during drift depends dramatically on the composition of the phase change memory alloy material. In this paper we add new data and interpretation on the resistance drift and its nature: a) Not only amorphous parts of device might be responsible for drift. b) Drift might be caused not only by the phase change but also by electrical switching, which in turn is the consequence of electronic high current density filaments appearance.

Key words: phase-change, chalcogenide, drift, and crystallizing-amorphizing

1. INTRODUCTION

In electrical phase-change memory (PCM or OUM) devices, the monotonic and continuous dependence of resistance on the programming current pulse or its falling edge creates a very large number of distinguishable states [1]. In reality the usefulness of this large number of states is limited in any multi-level cell (MLC) PCM product applications, by the continuous change of resistance with time after programming (drift). Thus a better understanding of the drift mechanism and its control is very important for any MLC applications.
In general there are many possible sources of resistance drift. These sources can include the change in resistance of the polycrystalline part of the device, or the change in resistance of any interfaces present inside the device (which include metal-vitreous chalcogenide and crystalline-vitreous chalcogenide interfaces), or the change with time of the resistance of the amorphous or vitreous parts of device [2]. Since all of these sources are inside each device, they are interconnected to each other and the visible drift comes from the dominant source.
The current point of view on drift could be formulated as follows: resistance of PCM is proportional to the volume fraction of amorphous phase and drift is associated with the relaxation of parameters of amorphous (or vitreous) phase only. Further support for this point of view can be found in experiments reported in [3] where it was shown that additional faster quenching changed “anomalous” drift of 225 devices into well-behaved devices following a power law. Though quite logical and seemingly correct this typical point of view of drift seems not applicable to Lower Resistivity Alloys (LRA) or for multilayered devices of 225 with LRA nearer the contacts. In these devices the maxima of drift was routinely observed at intermediate ranges of reset resistance (Fig.1). Thus if the increase of device resistance is due to the growth of volume fraction of amorphous material and it is valid for LRA, then we must admit that the drift maxima at intermediate resistance in devices containing LRA occurs for some other reason, despite the fact that the amorphous volume fraction continues to grow with resistance.
This contradictory situation is partially due to the fact that resistance drift of only one alloy 225 has received detailed experimental and theoretical study. Thus the aim of our investigation is to fill some gaps in the experimental knowledge base on resistance drift phenomena in PCM.

2. EXPERIMENTS

Most of the experiments were conducted on Ovonyx test stations using single square pulses (width ~100-200 ns) both for set and reset programming with a high series load resistor (4.5 – 10 KΩ) and minimal DC read voltage (0.1- 0.2 V).
The materials investigated were single-layer 225, LRA1, and multi-layer LRA2-225-LRA2 with various top electrical contacts (TEC). Most devices belonged to Ovonyx Technologies, Inc. produced by our in house Full-Flow (FF) process

on E-beam base coupons; a few came from Energy Conversion Devices produced by a breakdown (layer) process (BDL) with C – C contacts.
The following experiments were performed and data collected: drift exponent dependence on programmed resistance with different alloys for single-layered and multi-layered devices; drift exponent dependence on chalcogenide film thickness in single-layered devices; drift exponent dependence on temperature; resistance activation energy before and after drift for different alloys; and drift saturation and variation of its parameters with temperature.

2. RESULTS AND DISCUSSION

Drift exponent dependence on programmed resistance with different alloys single-layered and multi-layered devices.

After collecting drift data as resistance variation with time after a reset pulse, the data is summarized in the traditional way as:

$$R=R_o\,(t/t_o)^{d} \qquad (1)$$

where t_o is the time scale and R_o is the resistance at time $t = t_o$. With t_o = 1sec, the drift exponent was extracted and mostly the drift exponent (d) behavior will be presented in what follows.
Figure1 shows results of our study of drift in different alloys. As one can see the drift exponent in 225 peaks when the device resistance saturates at high reset levels. This seems to be natural as a reflection of the fact of stabilization of vitreous 225 at fast quench rates [3], which could be associated with higher programming currents. The first observation of d-Ro saturation at high R ignited more detailed study of high resistance drift in all alloys and devices we utilize and characterize.
Figure 1b shows drift in a single LRA1 layer device where the resistance drifts differently than in 225: at lower Ro drift is similar to 225 but the maximum drift exponent (d=0.075) is observed at an intermediate resistance value (~300K) and then falls to d ~ 0.04 for the highest reset resistance level (~1M) Also, the peak value is lower than for the single 225 layer. Now we have to understand why resistance continues to increase but drift exponent consistently (as measured in many devices) goes down after reaching a peak. To shine more light on the subject, in our next experiment we measured the same 225 alloy but layered between LRA2 (a more conducting GST alloy than LRA1). The 225 film was the thickest. Figure1c presents data typical for this type of device. To our surprise, despite the fact that device thickness was mostly comprised of the 225 alloy, the drift exponent was larger than 225, but the maxima appeared sooner than in LRA1, perhaps corresponding to the peak for LRA2 alloy.

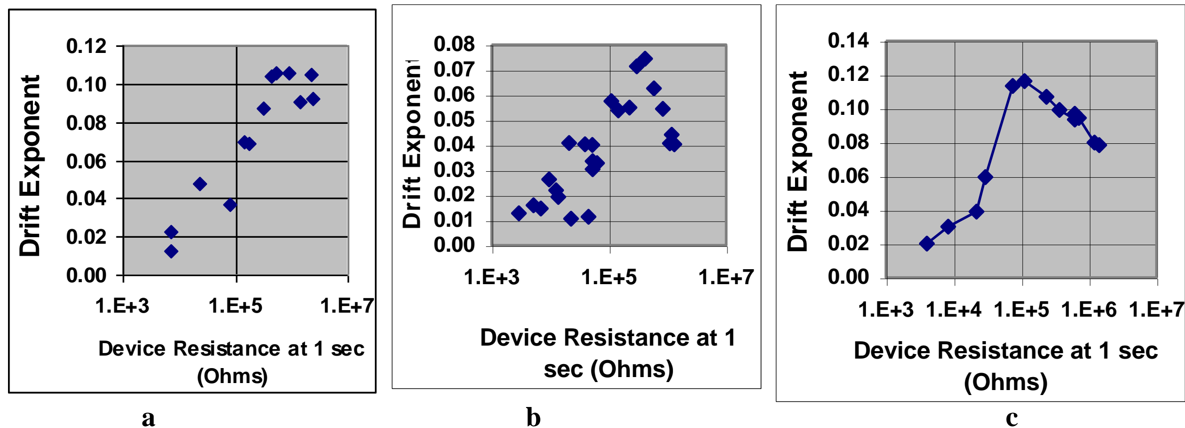
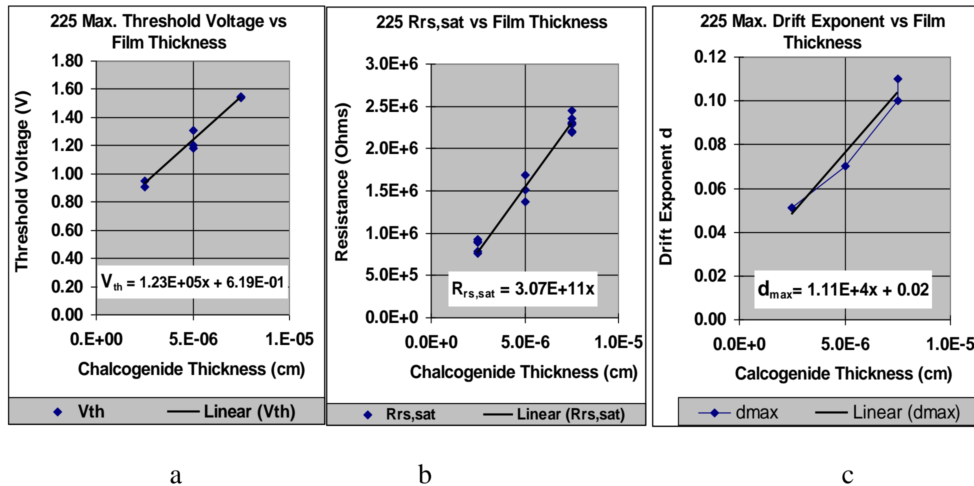


Fig.1. Drift Exponent with Different Initial Programmed Resistance. a) Single layered 225. 750A. b) Single layered LRA1. 750A, c) Multi-layered LRA2-225-LRA2.

We next study drift vs. thickness for single-layered devices of 225 and drift vs. temperature for LRA and 225 single and multilayered devices.

Drift exponent dependence on chalcogenide film thickness in single-layered devices

In this study GST 225 thicknesses of 250 A, 500 A, and 750 A on E-beam Full-Flow devices were used with TiAlN Bottom Electrical Contact (BEC) and Ti-TiN the top electrical contact TEC.
Figure 2a shows the threshold voltage of switching, 2b shows the saturated values of reset resistance, and 2c shows the drift exponent when plotted against the film thickness.



a b c

Fig. 2. Scaling of threshold voltage of switching (a), of saturated value of Rrs (b), and of max. value of drift exponent (c) with film thickness. 250A, 500A, and 750A 225 with Ti-TiN TEC.

From this figure it follows that all three parameters scale linearly with thickness. The approximate bottom contact area for these full-flow E-beam devices is 8E-11 cm^2. The spreading reset resistivity of 225 alloy calculated from the slope of the I-V curve appears to be 46 Ω cm, which is close to all previous estimates for this alloy. The interpretation of offset in Figure 2a suggests that it does not come from the bulk of the chalcogenide, and not from the bulk of reset region. If the assumption that only amorphous material participates in drift is correct drift rather comes either from the interface or from crystalline part of chalcogenide. We suspect that for LRA the latter plays a significant role. Therefore the next two sets of experiments are devoted to investigation of temperature effects in LRA1.

Drift exponent dependence on temperature

In the latest publications on drift, temperature is said to have a significant influence on drift. [4]. Unfortunately the experimental data presented in [4] was not for the drift exponent dependence on temperature during the drift, but rather for drift measured at RT for various annealing conditions. That is why higher resistance in [4] corresponds to higher temperature: well known fact of "revirginization" of device by annealing.

In Figure 3 we present data for the drift exponent against "real time" temperature during drift. For this experiment we programmed two LRA1devices (Fig.1b) to the right-hand side of the d-Ro curve, well after the maximum of d.

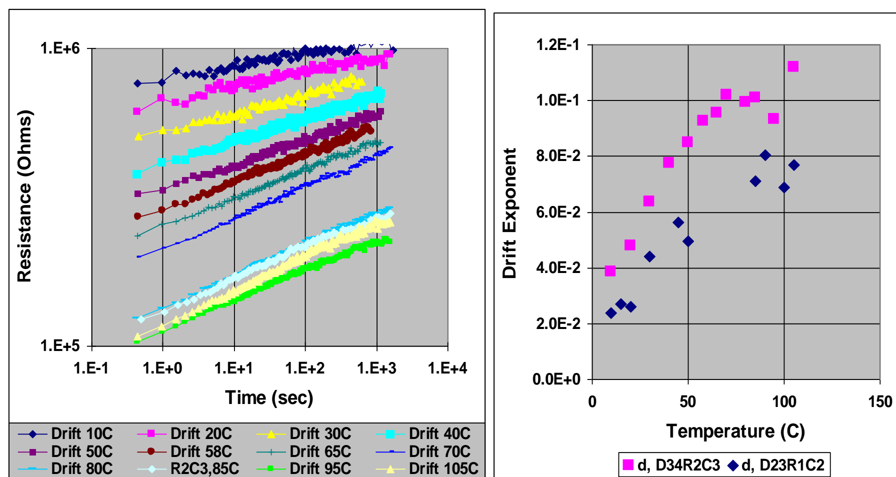


Fig. 3. Temperature dependence of drift for LRA1 E-beam full-flow devices with Ti-TiN TEC.

At maximum reset resistance of these devices, resistance drifts according to equation (1) with exponents 0.04 and 0.02 at 10C for both devices and both exponents grow with temperature 2 to 4 times. Between 70C and 90C the rise in d slows

down. If drift of Rrs,max in both alloys is due to the amorphous material present, measurements of resistance activation energy before and after drift would give us further insight in drift phenomena. The next paragraph describes this measurement.

Activation energy before and after drift for 225 BDL and for full-flow LRA1 devices

We compare here material property changes in Ea after short drift, observed while taking R-Is at different temperatures and Ea as measured after long drift of devices pre-programmed either at RT or at elevated temperature and drifted for a long time at elevated temperature On 225 BDL devices there were three resistance activation energy measurements - taken from R-Is at each temperature: Programmed at the right-hand end of R-I, Rdrifted at the very beginning of each R-I on the left hand side (resistance was drifted during the time between R-Is for approximately 10 sec), and Rswitched – resistance after switching at low current before device starts to set.

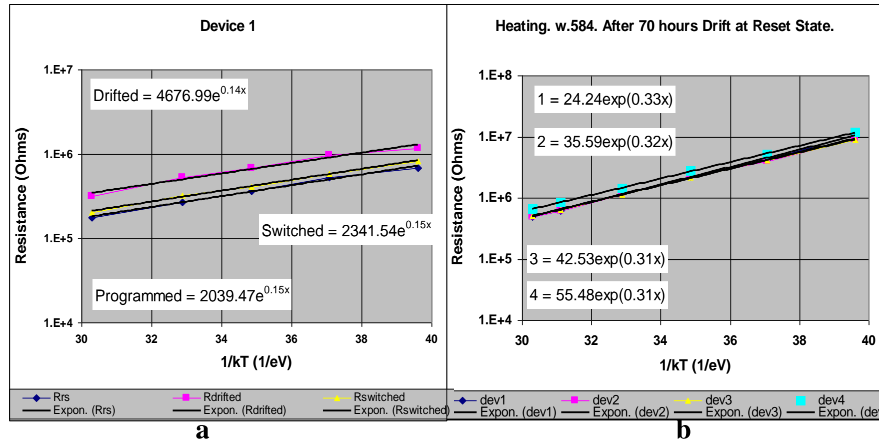


Fig.4. Activation energy of programmed resistance on different parts of R-I. for device 1 out of four (a) and of all four devices after long drift (b). Device 225 BDL with C-C contacts.

The resistance data is presented for four device in Fig. 4 vs 1/kT. After resistance drifting, the activation energy in Figure 4a did not change (but did drift not accelerate with temperature and did conductivity not increase with temperature? So saying that nothing changed may be incorrect.) but pre-exponential factor went up reflecting the change in density of states in mobility gap. Interesting that low-current non-programming switching restored the initial value of the prefactor, meaning that the density of states is changed back [8].

In the next experiment (Figure 4b) all four devices were programmed at high T, drifted for 70 hours at high T. RT data was taken before and after drift at elevated temperature. After long drift only resistance change with temperature was monitored and no R-Is were taken. The heating-cooling cycle was repeated twice to increase the certainty of the data and the data was averaged. This experiment shows that after long drift, resistance activation energy of 225 alloys goes up ~2 times and prefactor goes down. In Table 1 the data for activation energy before and after drift and after drift saturation (limited amount of data) were compiled for GST 225 and LRA1 devices, which were programmed to the maximum reset resistance. The data shows the drift of LRA1 effectively does not affect the activation energy.

Table.1. Resistance Activation Energy before drift (Rrs,sat from RI and initial resistance R_o from drift data) and after long drift or after drift saturation (Rsat).

	BEFORE DRIFT		*AFTER DRIFT*	
Alloy	**Ea,RI,bd (eV)**	**Ea,Ro,bd (eV)**	**Ea, ad (eV)**	**Ea, Rsat,ad (eV)**
225	**0.15**		**0.3**	
225	**0.21**		**0.35**	
225	**0.22**		**0.37**	
LRA1		**0.2**		**0.24**
LRA1	**0.19**		**0.2**	
LRA1		**0.16**		**0.13**
LRA1	**0.21**			**0.23**

From the above it follows that LRA presence has two consequences:

1. Maxima appears on d-Ro dependence at intermediate programmed resistances range, and
2. Activation energy change during the drift is much less pronounced in LRA than in 225.

Drift saturation with time and its variation with temperature.

Two sets of independent experiments were carried out. Several LRA1 devices were drifted for different times with different Ro. Rload was 4.5KΩ with 0.2V read bias. Devices were set to the same level before applying reset pulse. Set and reset pulses were 200ns. R-I-Vs and limited cycling was done on the first device. Others were reset and set several times. These devices were used because they showed very good stability and reproducibility. After drift monitoring was stopped, the coupon was removed from the test station and placed in an oven kept at 100C for ~ 14h. After annealing, the devices were re-measured for drift at RT for another 1000 seconds. The same procedure was repeated after another 72h at RT.

Drifts after 14 hr 100C anneal with additional (at Room Temperature) 24h, and 72h showed a clear tendency to saturate.

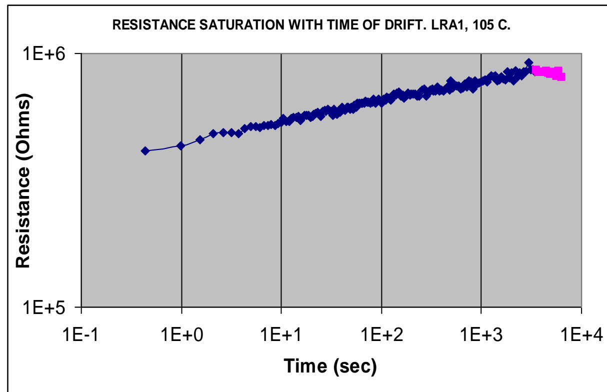


Fig. 5. Typical resistance drift saturation. LRA1, 105 C

Similar results were observed on several devices that were drifted for 1000 seconds, then were kept in the oven at 100°C for another 70h, after which they continued to drift at RT for 1000 sec, then again after 24h pause, and again after 72h. Table 1 shows the data for two devices that were subjected to a direct long drift on the hot-stage at different temperatures with 0.2V dc bias applied to them all the time. In LRA1 there is practically no difference in activation energy even after drift saturation. Because drift is an activated process and saturation time at room temperature would be too long (>1E5 sec), an attempt was made to get experimental dependence of time of drift saturation with changing temperature. The aim was to be able to predict drift saturation time for any alloy by testing it at 100C and extrapolating the time to room temperature. As was observed for several devices from LRA1 the temperature dependence of drift saturation time consists of two parts: the fast one with activation energy 1 eV at T > 85C and the slower one below 85C with an activation energy of 0.25 eV (Fig. 6). Extrapolation of the slow part of curve to 20C results in drift saturation time estimate of 1E5 sec very close to actually measured data. High value of activation energy is possibly due to band-to-band transitions at higher temperatures.

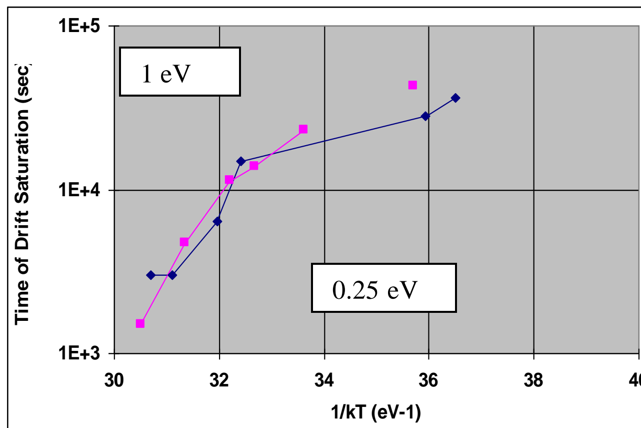


Fig. 6. Temperature Dependence of Time of Drift Saturation. LRA1 Full-Flow devices.

Drift elimination with low-current switching.

General comments on the drift elimination measurement technique using low current switching: drift elimination requires precise current control below programming conditions. This is most easily accomplished in a low capacitance environment and in a constant current regime such as available within an integrated circuit environment as opposed to a probe station.. Despite this limitation, our test were performed on a test station using ECD BDL devices with C-C contacts and dV/dI= 200-300 Ω with a 5 pF probe.

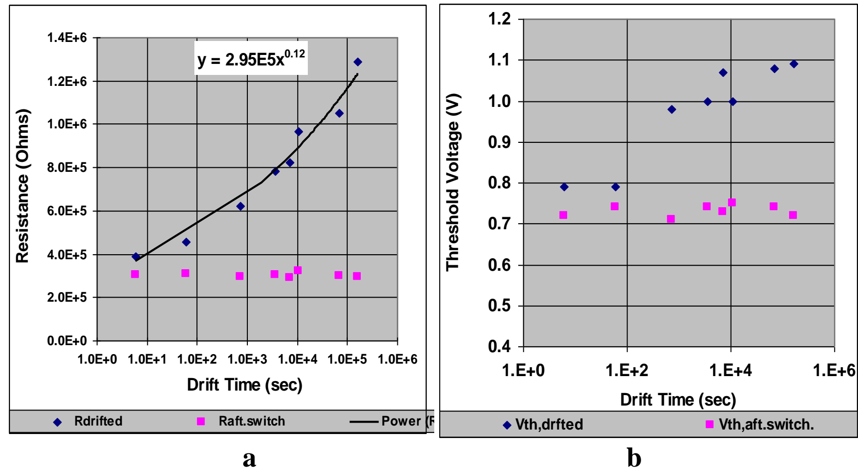


Fig.7. Low current switching eliminates drift of resistance (a) and of threshold voltage $V_{th,LEE}$ (b). 225 BDL devices with C-C contacts. Single reset level, 500ns pulse width

In this last experiment we compare $V_{th,LEE}$ -the threshold voltage on the leading edge of a pulse – used for drift reduction

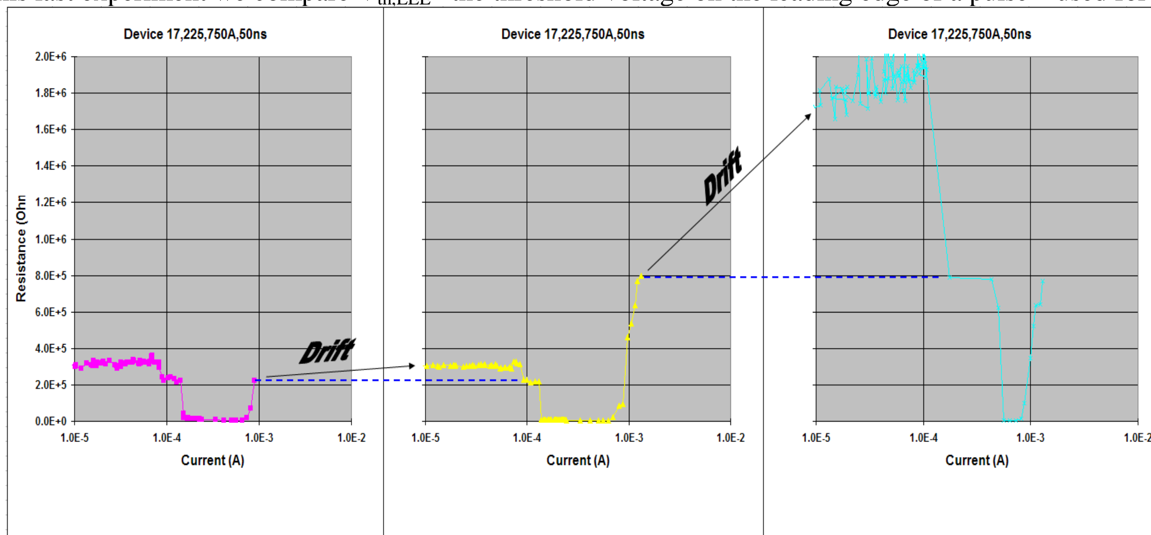


Fig. 8. Drift elimination. Programming Levels 200K and 800K, 50ns Pulse Width. 750A 225 ECD BDL devices.

Drift elimination has been shown to work with pulse widths ranging from 50 to 500ns at different programming levels (Rrs=40K – 5MΩ)and for different values of load resistors. From this experiment we have shown that low current switching is an effective way of resetting the drift clock.

Comments on the Nature of Drift
To our knowledge there are 4 known points of view on the nature of drift:
1. Change of the band-gap. From a comparative study of drift in optical parameters and the electrical parameters of deposited amorphous 225 films with time and temperature it was concluded that a small change in optical band gap (~ 0.01eV) could be responsible for the observed changes in reflectivity [5]. Rough estimates were done with expressions: for electrical resistance drift: $\delta Eel = kT*\ln(Rfinal/Rinitial)$ and it gave for amorphous films with silver paste contacts $\delta Eel = 0.018eV$. For optical data on films deposited on quartz carriers we used an expression for reflectivity (λ): $\delta Eopt = 1.24*\delta\lambda/(\lambda 1*\lambda 2)$ and it yielded $\delta Eopt = 0.0105eV$. Thus 0.01 – 0.02 eV change (with constant prefactor) is enough to explain both reflectivity and resistance change with time in 225 films and devices.
2. Change in atomic dynamics using the concept of double-well atomic potentials in glasses relates the observed parameter drift to the inherent structural relaxations (aging phenomena) in a glass, in the course of which a metastable glass structure relaxes to its more stable state [6]. Correspondingly, no new model is needed at all to understand the drift, which is related to the well-known structural relaxations in glasses summarized in the double well potentials (DWP) concept. In particular, understanding of the drift phenomena does not require any 'electronic' hypotheses. The DWP concept introduces a multitude of random atomic barriers underlying the exponentially broad spectrum of structure relaxation times. The structural relaxations change the specific volume that affects the threshold voltage and, through the deformation potential, changes the Fermi energy and resistance. The DWP model predicts the observed drift and its saturation, which is explained by the existence of the maximum barrier in the system. Simple analytical expressions show that, before saturation, the threshold voltage and the off state resistance drift proportionally to the logarithm of time and power-law dependence on time respectively [6].
3. Change in electronic configuration inside the mobility gap namely electron recombination and trap kinetics. [7]
4. In [4] it is stated that the following takes place in GST: (a) hopping electronic transport where (b) hopping occurs between the defects whose concentration is temperature dependent, and (c) defect annihilation times are thermally activated with uniformly distributed random barriers.
In this paper we offer a fifth possible point of view on the nature of drift; Drift in electrically programmed PCM is not caused by phase change, but due to stress from electrical switching.

4. Conclusions

The observed drift exponent maxima at moderate reset resistance value suggests that drift cannot be explained exclusively as a property of fully amorphous material.
The change of drift exponent with the chalcogenide film thickness could be explained by the fact that thin films can more easily adjust to stresses.
Low current switching reinitializes drift of resistance. This implies that electrical switching introduces stress and switching reintroduces initial stress in a relaxed, drifted device.
Drift is caused not by phase change itself but is a consequence of electrical switching, which in turn is related to electronic high current density filaments..
Resistance drift saturation was observed for all LRA1 devices tested.

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Biographies

Sergey Kostylev was born in Dnepropetrovsk, Ukraine. Received B.S. and M.S. in physics and mathematics and Ph.D. in physics of semiconductors and insulators (PSI) from Dnepropetrovsk state university, Ukraine in 1959 and 1966 respectively and Doctor of Science in PSI from Moscow Institute of Radio-electronics and Engineering of Academy of Sciences of USSR and the Highest Qualifying Commission of USSR in 1982.

1991 Institute of Technical Mechanics of the Academy of Sciences of Ukraine, Dnepropetrovsk. Head of the Department of Semiconductor Electronics. Principal investigator for more than 20 projects in fundamental and applied physics of electronic instabilities in a media with a bulk N- and S-type Negative Differential Conductivity (NDC). GaSb.

1991 -1999 Energy Conversion Devices, Inc., Troy, MI, USA, Senior Research Scientist; Development of Chalcogenide High-Speed Multistate Ovonic EEPROM. 1999-2008 Ovonyx, Inc, Rochester Hills, MI, USA. Principal Research Scientist. Development and optimization of Ovonic Unified Memory (OUM) and OTS. Published (in co authorship) 3 books (on electrical switching in amorphous semiconductors, on Gunn-effect devices and on interlayer interaction in multilayered structures with S- and N-type NDC), more than 200 papers and patents.

Tyler Lowrey, President, Chief Executive Officer and Director – Ovonyx, Inc.

Mr. Lowrey has overall responsibility for the Company and its projects, alliances, outside investors, investments and day-to-day operations. The Company is chartered with commercializing chalcogenide phase-change nonvolatile memory devices (“PCM”). He is the inventor/co-inventor of more than 100 U.S. patents related to semiconductor memories and more than 60 OUM-related patent disclosures. Mr. Lowrey has an extensive background in solid-state IC memories and their development, debug and ramp-up to high-volume competitive production. He served as a process engineer and device engineer and in mid-level and senior-level management positions at Micron Technology, a Fortune 500 memory producer. While at Micron, he was Vice President-Chief Technical Officer and Vice President-Chief Operating Officer as well as a director and Vice Chairman of Micron’s board of directors. As part of the Company's joint development programs with the Company's licensees, Mr. Lowrey assists to evaluate, debug and optimize the processes, materials, devices and cell structures – with particular attention to processes and electrical characterizations. Mr. Lowrey is presently on the Board of Directors of Litel Corp.