Compact Electro-Thermal Model for Thermal Cross-talk Analysis in PCM Arrays

Aravinthan Athmanathan[1,2], Abu Sebastian[1], Daniel Krebs[1], Milos Stanisavljevic[1], Yusuf Leblebici[2] and Evangelos Eleftheriou[1]
[1]IBM Research – Zurich, 8803 Rüschlikon, Switzerland
[2]Ecole Polytechnique Fédérale de Lausanne (EPFL), 1005 Lausanne, Switzerland
aat@zurich.ibm.com

ABSTRACT

Phase change memory (PCM) is one of the frontrunners among the emerging non-volatile memory technologies. Even though a Joule-heating-induced phase change mechanism has been demonstrated down to a few nanometer dimensions, a key factor that could possibly limit the scaling trends in a PCM memory array is the thermal cross-talk between adjacent cells. In this article we present a compact electro-thermal model for investigating potential thermal cross-talk issues in highly dense PCM arrays. The proposed model can be used as a simple yet powerful tool to perform the otherwise computationally intensive thermal analysis for the PCM array using finite element modeling approaches. Besides providing an accurate measure of spatial and temporal thermal variations across the cell, this modeling approach can also provide insights for the PCM cell design, scaling aspects as well as solutions to mitigate the thermal crosstalk problem.

Key words: Phase Change Memory, Thermal cross-talk, Compact modeling, etc.

1. INTRODUCTION

Phase Change Memory (PCM) technology has evolved as a promising candidate for future non-volatile memories (NVMs) [1]. Besides the potential for low-power and high-bandwidth operation as well as high endurance, a key advantage of PCM technology is thought to be its scaling potential. However, a critical challenge to the scaling road map of PCM technology is the issue of thermal cross-talk. Thermal cross-talk refers to the unintended thermal interference between a PCM cell that is being programmed and its adjacent cells in a memory cell array. Earlier studies indicated that the scalability of PCM looks promising from a thermal crosstalk perspective; however, when considering the current scenario of scaling trends and device geometries, investigating thermal cross-talk is critical especially for technologies below the 20 nm node. In this article we present a 3-D compact electro-thermal model (CETM) for modeling the thermal cross-talk between the cells in a highly dense PCM array. We propose a simple yet powerful approach to get a fast and accurate estimate of the spatial and temporal temperature variations of the cell without employing the computationally intensive finite element modeling (FEM) based approaches.

2. EXPERIMENTS

There is an electrical and thermal component associated with the programming of a PCM cell as indicated in Fig. 1(a). Figure 1(c) shows the typical IV characteristic corresponding to a PCM cell in the SET and RESET states. During programming, the field is high enough so that the cell is in the so-called “ON” state and the corresponding resistance is denoted by “ON” resistance. When the current flows through the PCM cell, there is substantial Joule heating and power is dissipated within the cell. This power is mostly determined by the “ON” resistance of the PCM material. In typical confined cell geometries (Fig. 1(b)), larger part of the power is dissipated within the phase change material. The dissipated power will heat up the nanometric volume of phase change material to very high temperatures. The region where the peak temperature is reached is referred to as the “hotspot”. During a RESET process, the temperature at the hotspot could be much higher than 1000 K. Note that to melt and subsequently amorphize the PCM material, the temperature within the cell should be higher than the melting temperature which for GST is typically around 900 K.

Aggressive scaling, particularly in a $4F^2$ array configuration, the cell pitch reduces correspondingly. On the other hand, the temperatures reached within a PCM cell do not scale with device dimensions. Hence, there will be increasing thermal interference between a PCM cell that is being programmed and its neighboring cells. This problem is commonly referred to as thermal cross-talk. This is a significant problem and has triggered significant research effort in recent years [2, 3]. Finite element modeling approaches are popular in the study of PCM cell operation. However, they are typically computationally intensive and provide less intuition than simpler compact models [4]. For array level studies, FEM tools are even less attractive and hence, there is a need for a simpler modeling approach. We propose a compact electro-thermal model, which is simple and can give accurate estimates of the spatial and temporal thermal variations across a PCM cell array. Interdependent electrical and thermal sub-models constitute the CETM. In CETM approach, each PCM cell can be divided into elements based on its components (electrodes, phase change material, insulating layer) and typical geometries like cuboid, cylinder, etc. The electrical sub-model consists of a simple resistive network representing the electrical resistance of each conductive element including the "ON" field resistance of the PCM. For an applied voltage, the electrical sub-model yields the current flowing through each element and hence the power (P_{th}).

The thermal sub-model uses a simple thermal equivalent electrical circuit for each element to obtain the heat flow and temperature distribution throughout the cell at the specified node points. The well-known analogy between heat flow and electrical conduction is applied in the thermal sub-model with the temperature represented as voltage and the heat flow represented as electric current. In the thermal sub-model, each element can be modeled as a node containing thermal resistances representing its resistance to heat flow, thermal capacitance representing its ability to store heat and a current source to represent the source of heat. The temperature map from the thermal sub-model can then be used to determine the location of the "hotspot". To evaluate the temperature distribution within an array, these nodes are repeated along with the respective nodes for the insulation barriers and the metal interconnects.

3. RESULTS & DISCUSSION

To validate the accuracy of the CETM approach, the thermal cross-talk analysis is performed on representative confined cell architecture [5]. The switching voltage for programming can be evaluated between these sub-models in a few iterations until the peak temperatures at specific nodes reach above the melting temperature of the PCM. In the studied cell architecture, the peak temperature occurs in the center of the cell, spatially represented by the node of the PCM element. Incase of asymmetrical cell geometries where the peak temperature occurrence is not at the center, we can break down the PCM element into a few more elements, in order to find the spatial location of the peak temperature. The input power is calculated such that the temperature at the PCM boundaries is greater than the melting temperature of 900 K, to make sure that the cell is RESET to high resistance. The CETM can be implemented and simulated in SPICE/Spectre like simulators. The results are compared with the 3-D FEM-based simulation results obtained in COMSOL (Fig. 4). The results show good match between the CETM and FEM simulations. In CETM(1), the entire PCM component is modeled as a single element whereas in CETM(2) it is divided into two elements.

To illustrate an application of CETM approach, a scaling study is presented. A high RESET pulse is applied to program the cell and the thermal cross-talk on adjacent cell is evaluated. T_{dist} denotes the temperature variations of the disturbed cell at the nearest boundary to the cell being programmed (inset of Fig. 5a). The T_{dist} is studied for different cell pitch dimensions, with normalized input power, in order to obtain the same peak temperature. In order not to disturb the adjacent cell, the temperature T_{dist} should be significantly below the crystallization temperature of the phase change material, typically in the range of 460 K-500 K [3]. For the cell under investigation, T_{dist} exceeds this critical temperature when cell pitch dimensions are smaller than 20 nm. To explore the possibility of bringing down this temperature for 20 nm cell pitch dimension, T_{dist} is evaluated for various thermal conductivities of the thermal barrier layer (BAR in Fig. 1b). This is illustrated in Fig. 5b. The results imply that for barrier layer with thermal conductivities less than 0.3 W/mK, T_{dist} falls below the temperature range of fast crystallization.

4. CONCLUSION

We proposed a compact electro-thermal model for investigating thermal cross-talk issues in highly dense PCM arrays. The scaling studies presented also illustrate the effectiveness of this modeling approach. The inherent simplicity and speed of simulation make this model a powerful tool for providing insights into the thermal characteristics of a PCM cell array and in particular for addressing thermal disturb. The model can also be used to evaluate the PCM cell and array designs that mitigate thermal interference. The effects of altering the thermal properties of materials, the device geometry and the addition of thermal insulating barriers can be readily studied using this model.

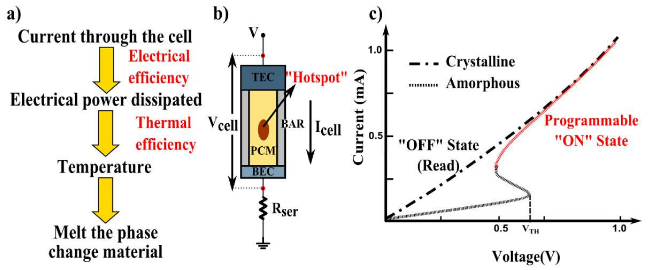

Fig. 1. a) Schematic representation of the RESET programming; b) Hotspot location in a generic confined cell topology; c) IV curve showing the programmable "ON" state.

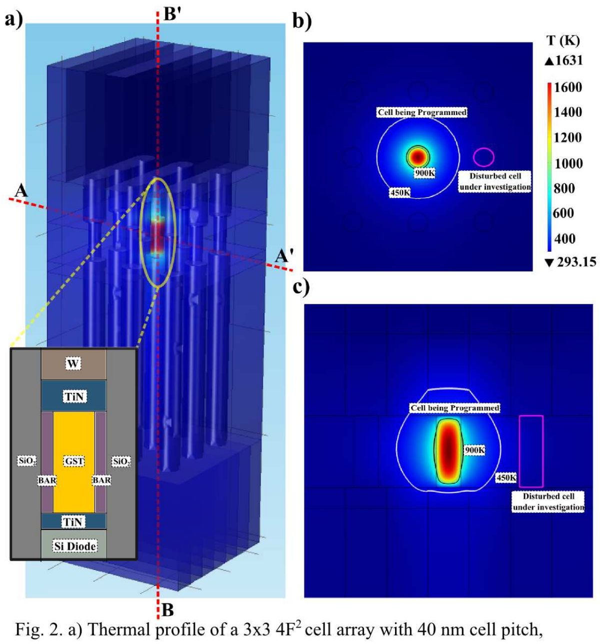

Fig. 2. a) Thermal profile of a 3x3 $4F^2$ cell array with 40 nm cell pitch, implemented as 3-D model in COMSOL; b) Cross-section along the AA' plane showing temperature map while programming; The contours represent the melting and crystallization temperature; c) Thermal map along the BB' plane showing the cell being programmed and the disturbed cell.

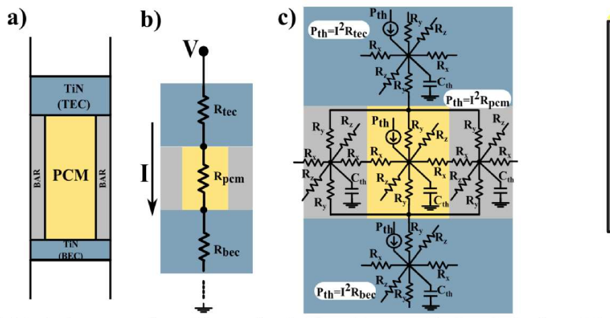

Fig. 3. a) Vertical cross-section of the confined cell architecture; b) Electrical sub-model for P_{th} calculation; c) Thermal sub-model circuit for a temperature profile evaluation.

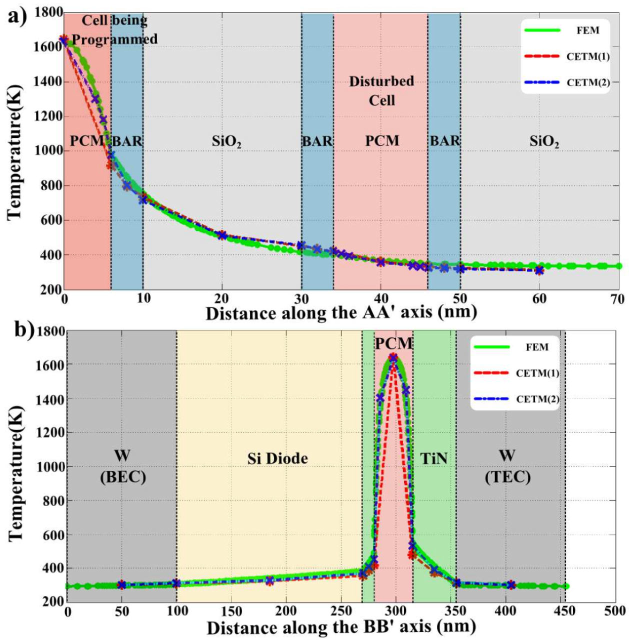

Fig. 4. a) Temperature profile along the AA' axis from Fig. 2 showing the temperature map across the cell being programmed and the disturbed cell; b) Temperature profile along the BB' axis from Fig. 2 showing the temperature map along the axis of the cell being programmed.

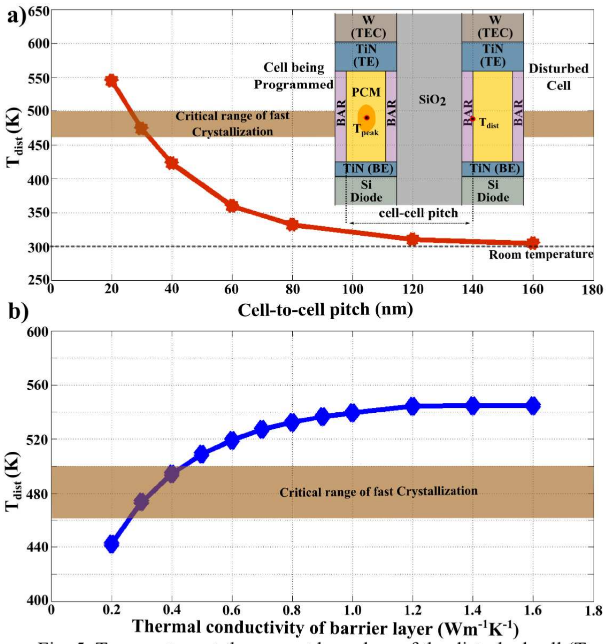

Fig. 5. Temperature at the nearest boundary of the disturbed cell (T_{dist}) a) vs the cell pitch dimension; b) vs the thermal conductivity of barrier layer

REFERENCES

[1] H.-S. Wong et al., "Phase change memory," Proceedings of the IEEE, vol. 98, no. 12, pp. 2201–2227, 2010. [2] S. Kim et al., "Thermal disturbance and its impact on reliability of phase-change memory," in IRPS, 2010 IEEE International, pp. 99–103, 2010. [3] U. Russo et al., "Modeling of programming and read performance in phase-change memories" Electron Devices, IEEE Transactions on, vol. 55, no. 2, pp. 515–522, 2008. [4] A. Pantazi et al., "Multilevel phase change memory modeling and experimental characterization" in EPCOS 2009, pp. 34–41, 2009. [5] I. S. Kim et al., "High performance PRAM cell scalable to sub-20nm technology with below $4F^2$ cell size" in VLSI Technology (VLSIT), 2010 Symposium on, pp. 203–204, 2010.