Lateral design for phase change random access memory cells with low-current consumption

P. Haring Bolívar, F. Merget, D.-H. Kim, B. Hadam and H. Kurz
Institute of Semiconductor Electronics, RWTH Aachen University, Sommerfeldstr. 24, 52056 Aachen, Germany.
e-mail: haring@iht.rwth-aachen.de

Abstract: Phase-Change RAM (PCRAM) is an attractive non-volatile memory technology which bears a large potential to become the unified solution for the miscellaneous demands of the future memory market. Lowering the large current requirement during set/reset operations is one of the most critical issues of future PCRAM technology. Not only the coverage of the mobile applications market but also the scalability and integration into high-density integrated memory demand a significant reduction of current and power consumption. In this paper we present an innovative lateral phase-change random access memory (PCRAM) cell design featuring advanced geometry and thermal management, thereby reducing power consumption during set/reset operation. The fabrication and work principle are described. Basic set- and reset-operation is demonstrated and compared to numerical simulations.

1. INTRODUCTION

Our information society at the turn of the 21st century bears a huge demand for microelectronic devices with drastically enhanced performance, in order to fulfill the society's future requirements for information processing, transfer and storage devices. One of the most dynamically evolving sectors of microelectronics is currently the non-volatile memory market, which is perceived by the consumer in the pervasive memory sticks, memory cards for digital cameras, etc... Currently the preferred solution for the non-volatile memory sector are floating gate memory devices (FLASH memories). However, scalability limitations of this concept compel for alternative solutions in the coming years. Three candidate technologies are currently competing to be the next generation solution for the non-volatile memory market. One of the most promising candidates are phase change random access memories (PCRAM) or *ovonic* memories, where changes of the crystallographic phase (amorphous or crystalline) of chalcogenide materials are used to store bits of information, given the high resistivity contrast of the different phases. This concept has many advantages with respect to scalability, processability and compatibility with established manufacturing procedures. However, one of the most critical remaining problems is the relatively large current consumption of existing PCRAM concepts, which is extremely problematic in view of future scaling limitations towards ultrahigh density memory solutions. In this presentation we present a new PCRAM concept, which addresses this critical issue and shows the path towards memories with a drastically reduced current consumption.

2. THE LATERAL PCRAM CONCEPT

The conventional "vertical" PCRAM cell design has the active phase-change material sandwiched vertically between two metal electrodes (or between a metal and a "resistive heater") [1]. Electrical current flows in a vertical direction. The current requirement of a PCRAM cell is dominantly defined by the area through which current flows. In a vertical concept this area is unavoidable defined by F^2, taking F as the minimum lithographic feature size, which leads to a large current consumption regarding to the current drivability of CMOS transistors at the same lithographic feature size. Additionally, the direct contact of the metal contacts with the switching zone of a vertical PCRAM cell causes a too large heat dissipation via the metal contacts during switching operations, further enhancing the current density needed to achieve phase change. This is unavoidable as long as the metallic contacts are in direct contact with the actively switching region of the phase change material, as the Einstein relation between heat conductivity and electrical conductivity unavoidably couples the high conductivity required to contact the material effectively with a small series resistance with a large heat dissipation. Alternative PCRAM concepts to minimize current consumption are therefore intensely sought after [2]. Attempts to minimize heat dissipation are mostly based on using a thermally less conducting contact ("heater") in an asymmetric cross-section configuration to switch only at the heater contact.

The novel lateral cell concept presented here (Fig. 1), has the active phase change material aligned *laterally* between the two metal contacts with a lateral constriction defining the active switching zone. This new approach has several advantages. On the one side, as the current flows in a lateral direction through the phase change material layer of thickness t, the current defining area is drastically reduced to $F*t$, as layer thicknesses t can easily and controllably be

manufactured to sizes significantly smaller than *F*. As an order of magnitude estimate, phase change layers of thicknesses smaller than 6 nm have repeatedly shown to exhibit stable phase change operation capabilities, while lithography sizes F are still on the range of 90nm. Thinning of the active layer in the active switching zone can additionally be used to further reduce the switching current. An additional advantage of a lateral concept is that the switching zone is defined by a constriction in the PC material itself, well separated and thermally decoupled from the metal contacts. These effects reduce current requirements significantly, as the heat dissipation can be set to values smaller than the situation in a vertical memory cell. In order to adjust the heat dissipation to the values required by the amorphization step ("reset") requirements, a separated heat sink layer is introduced below (or above) the active switching region to regulate the heat dissipation. This effectively decouples electrical design (determined by the lateral shape and thickness of the active phase change layer) from the thermal design (determined by the thickness of a heat conduction and heat sink layer below the active structure) of a PCRAM memory cell, opening the path towards further design optimization. In the traditional vertical PCRAM cell, heat dissipation and electrical conduction occur in the same spatial direction, coupling both effects and leading to trade-off situations in the design of a memory cell.

3. CELL FABRICATION

The fabrication of a lateral PCRAM cell is simple and based on standard CMOS fabrication techniques (sputter deposition, pattern definition by EBL / optical lithography, pattern transfer by RIE) and can easily be added on the CMOS process flow at the position of the first metallization layer above a previously manufactured CMOS layer. In the exemplary structures demonstrated here, only isolated, individually contacted memory cells on a flat Silicon wafer acting as a natural heat sink are manufactured in order to simplify fabrication procedures. The processing starts with the layer deposition of the complete layer stack on the silicon wafer by sputtering the heat conduction layer made from ZnS:SiO2, the phase change material ($Ge_2Sb_2Te_5$) and the evaporation of the contact metal (Ti or TiN). After layer deposition, the perimeter of the memory cell is structured via ion-beam-milling down to the silicon substrate. A second E-beam lithography step is used to define the trench between the metal contacts, and again the trench is structured by ion milling. Fig. 2 shows an SEM micrograph of the switching zone of a lateral PCRAM at this processing step. The cells are finalized by a SiO2 passivation and fabrication of metal contacts for external contacting.

4. MEASUREMENT AND TESTING

In order to show basic functionality of the lateral cell design static, dynamic and cyclability measurements are performed on such single cell structures (DUT). The static I-V measurements incorporate a pulsed reset-operation (short, intense amorphization pulse) and a static set during current controlled I-V measurement. The dynamic measurement incorporates pulsed set- (long, weak crystallization pulse) and reset-operation. For cyclability measurement alternating set- and reset pulses are applied to the DUT.

5. DISCUSSION

Fig 3 shows the result of an illustrative static switching experiment. The initial status of the switching zone of the DUT is crystalline. A resistance $R_{SW,c} = 51k\Omega$ is derived from a static, current controlled I-V measurement. A reset-pulse of 1V for 50ns is applied, causing the amorphization of the switching zone. A resistance value of $R_{SW,a} = 2M\Omega$ is determined for the amorphous state. The static I-V measurement caused the DUT to switch back into the crystalline state at a current of only 3.3µA (static "set"). A subsequent static I-V measurement validates the crystalline state of the switching zone ($R_{SW,c} = 54k\Omega$). These values agree with simulations. Current is extremely low in comparison to published PCRAM data. The contrast between the resistance values is greater than 100 and thereby more than sufficient for device operation. Taken the resistance value of the crystalline state one can estimate the total current drawn by the cell during the reset-operation to be less than 100 µA at W=200nm. Compared to published data of vertical cells (I = 1mA) with similar dimensions at a feature size of 180nm [3], shows the large potential of the lateral cell concept for a significant reduction of switching current. This concept shows advantages even in comparison to edge contact approaches recently demonstrated [2].

6. CONCLUSIONS

This paper presents a novel lateral PCRAM cell design, which allows an effective reduction of switching current during set- / reset-operation down into the µA regime. It shows thereby its potential for high and highest integrated non-volatile memories in order to meet the expectations of future microelectronics technology nodes.

Acknowledgement
We gratefully acknowledge V. Giraud and P. Gaud for layer deposition and EC financial support under IST-2001-32557.

REFERENCES

[1] S. Lai and T. Lowrey, "OUM – a 180nm cell element memory cell technology for stand alone and embedded applications", IEDM 2001.
[2] Y.H Ha, J.H. Yi, H. Horii, J.H. Park, S.H. Joo, S.O. Park, U-In Chung and J.T. Moon, "An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption", VLSI Symposium 2003.
[3] S. Lai, "Current status of the phase change memory and its future", IEDM 2003.

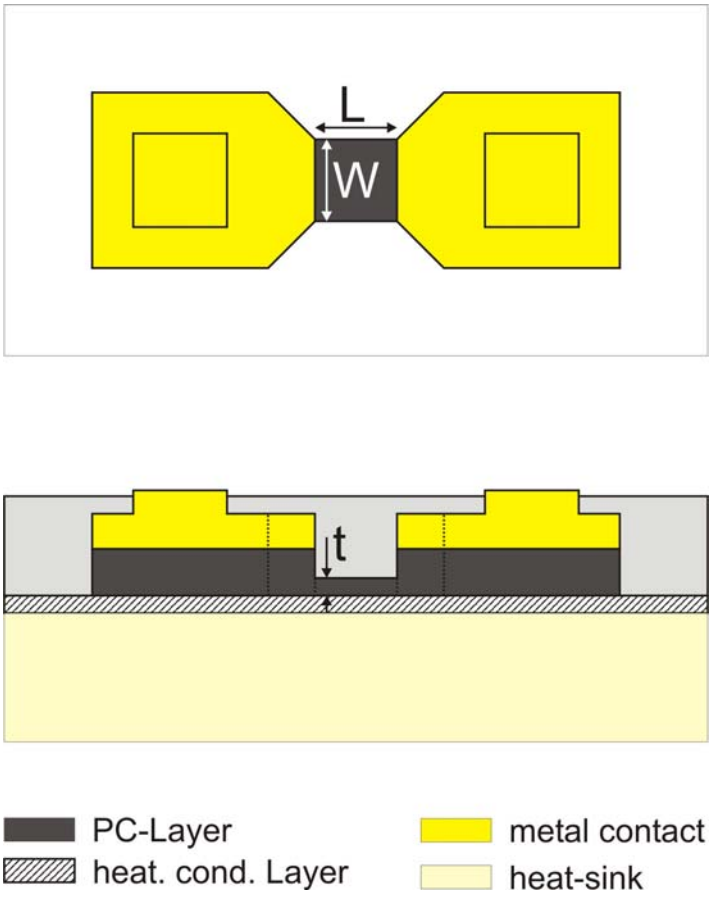

Figure 1: Schematic view of simplified lateral PCRAM cell. Upper graph: Top-view of lateral constriction within the phase change layer defining the switching zone width (W). The operation voltage is defined by the distance between metal contacts (L). Bottom graph: cross-sectional view showing how the phase change layer (PC-layer, dark) is thinned (t=thickness within the switching zone)

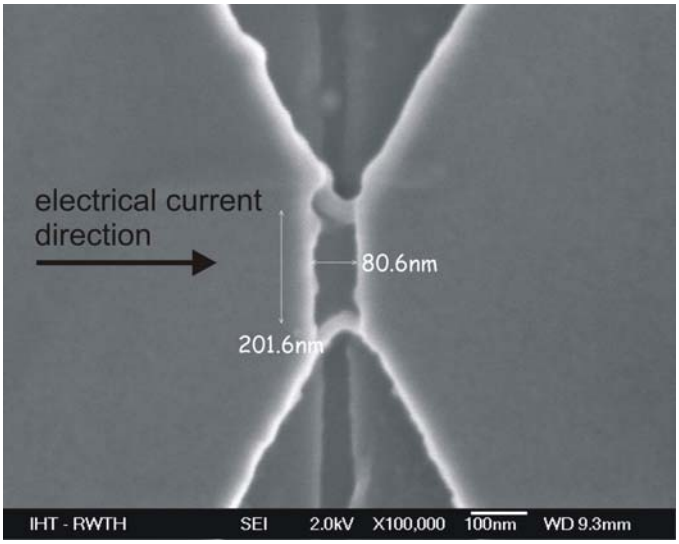

Figure 2: SEM micrograph of switching zone of lateral PCRAM cell test structure. Current flows in the lateral direction from the V-shaped contacts into the constriction area which is switched by current pulses. The current cross section is defined by the constriction width W=200nm and the thinned switching layer thickness t=25nm. The switching voltage by the length L=80nm of the constriction in the current direction.

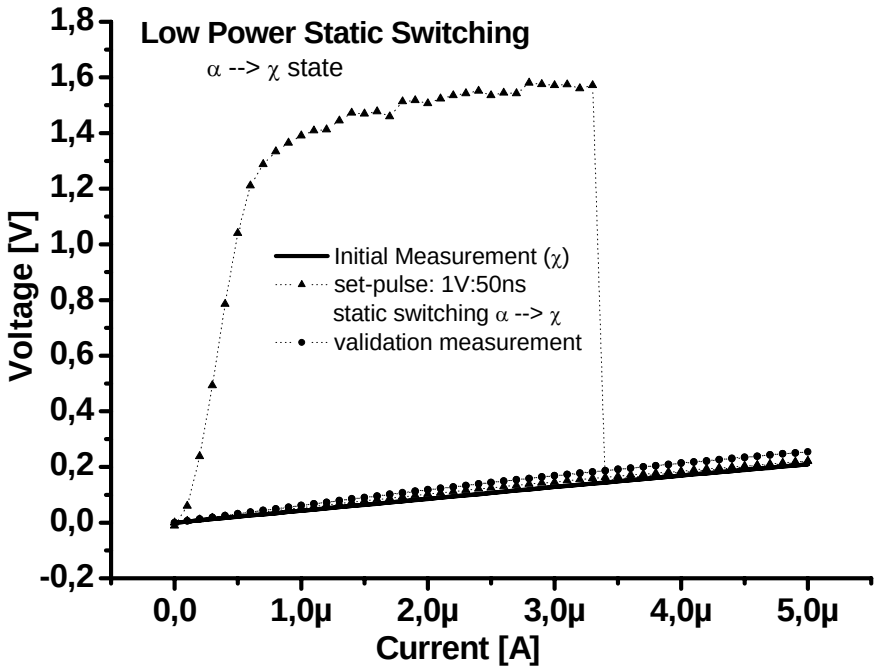

Figure 3: Low power static switching experiment with lateral PCRAM cell, showing the static I-V characteristic before test (straight line), after application of a 1V 50ns pulse (triangles) and after recrystallization (diamonds). The triangle data shows the static recrystallization at approximatedly 3.3 µA as a sharp reduction of voltage.