# Development Lines for Phase Change Memory

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**Introduction** — Industrial exploitation of chalcogenide materials is in place since many years in the optical field for the rewritable compact disk applications. As a consequence the research and development efforts have been focused in this direction, mainly studying the optical behaviors [1].

Only recently the use of chalcogenide materials to realize Phase Change Memory (PCM) has been proposed with the aim to have high performances and high density semiconductor Non-Volatile Memory (NVM) [2]. Although the PCM concept has demonstrated to be very solid and the PCM technology has reached very good maturity level [3], the introduction in the memory market has not yet happened. The main reason is related to the continuous scaling of the industry standard memories, both DRAM and Flash, well beyond what was forecasted. In particular the Flash memory has now surpassed DRAM at the leading edge technology node, becoming the technology driver of the semiconductor memory industry. Nevertheless the development of PCM is constantly increasing with the aim to become a mainstream technology.

For this reason there is a constant intense effort on the PCM technology development, on the chalcogenide material characterization and in general on the exploration of new alloys. On the first there is mainly the focus of the semiconductor industry with the constant improvements of the process integration. On the second there is mainly the focus of the academic and research centers. In the following the main development lines adopted for the process integration and for the chalcogenide materials exploration are briefly sketched.

**Process Integration** — The Phase Change Memory (PCM) cell is essentially a resistor of a thin-film chalcogenide material with a low-field resistance that changes by orders of magnitudes, depending on the phase state in the active region. For semiconductor industry application the most interesting material used so far is the $Ge_2Sb_2Te_5$ alloy which follows a pseudo-binary composition (between GeTe and $Sb_2Te_3$), hereafter referred as GST. The switch between the two states occurs by means of local temperature increase. At temperature just below melting, the crystal nucleation and growth occur and the material becomes crystalline (Set operation). To bring the chalcogenide alloy back to the amorphous state (Reset operation), the temperature must be increased above the melting point of hundreds of °C and then very quickly quenched down in order to preserve the disorder and not let the material to crystallize. From an electrical point of view, it is possible to use the Joule effect to reach locally both critical temperatures using the current flow through the material by setting proper voltage

pulses. Programming thus requires a relatively large current, in order to heat-up the GST and lead to a thermally induced local phase change. Phase transitions can be thus easily achieved by applying voltage pulses with different amplitudes and with durations in the range of tens of nanoseconds. The cell read out is performed at low bias. Since the two phases present a different resistivity, the logic 1 and 0 are defined as the low (crystalline) and high (amorphous) one, at which correspond respectively high or low reading current.

Considering the electronic and transport properties of the GST alloy, either in the crystalline or in the amorphous state, in order to form a functional compact cell array, a PCM cell must be formed by the variable resistor (heater and GST – called data-storage) with in series a selector device (transistor). Hence, the basic PCM cell has a 1Transistor/1Resistor structure. The type of transistor and of data-storage varies respectively as a function of the application and of the process architecture strategy. For high-density memory, a more compact cell layout is achieved via the vertical integration of a *pnp* bipolar transistor [4], while for embedded memory the transistor is a n-channel MOS, where a larger cell size is balanced by a minimum process cost overhead with respect to the reference CMOS.

The integration of the data-storage occurs between the front-end and the back-end of the CMOS process. The "simple" variable resistor, i.e. the heater and GST system, may be obtained in different ways and the choice is a function of the understanding of process complexity, current performances, thermal properties and scaling perspective [5]. A possible approach is to use a sub-litho contact heater with a planar GST [6] or a modified version with a recession in the contact and GST confinement, which should improve the thermal properties and hence reduce the reset current [7-11]. A completely different approach relies on the definition of the contact area between the heater and the GST by the intersection of a thin vertical semi-metallic heater and a trench, called "μtrench" [4, 12-13], in which the GST is deposited. The μtrench architecture keeps the programming current low and maintains a compact vertical integration. Since the μtrench can be defined by sub-litho techniques and the heater thickness by film deposition, the cell performance can be optimized by tuning the resulting contact area still maintaining a good dimensional control.

Since PCM technology is based on the basic properties of the chalcogenide alloy, the integration of the material into a standard CMOS process still represents a challenging matter: not for the single cell concept, already proven to be very strong, but for the manufacturability of very high density NVM, where the technology can be considered robust only if demonstrated only over many billions of cells. Another critical topic is represented by the reset current: its controllability and reduction is fundamental to guarantee a compact and scalable cell size, a competitive writing power consumption and enhanced reliability. Hence the development efforts are mainly focused on the optimization of the data-storage structure with respect to the reset current. Recent results have shown good improvements both in the robustness of the process integration and in the cell current reduction with the perspective of a continuous scaling according to the technology node [10, 12-14].

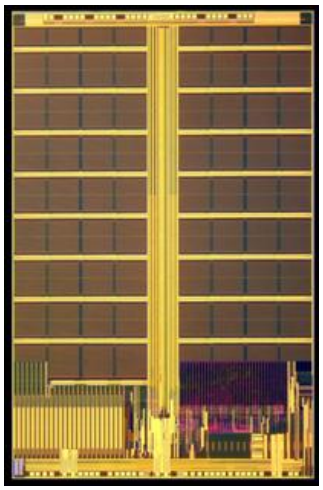

Fig.1: 128Mb Phase Change Memory Device [12, 15].

The PCM technology has reached the phase of product demonstrator [12, 15], with a 128Mb device sampling (fig.1) showing fast growing capabilities to reach the maturity for manufacturability.

**Material Exploration** — As reported in the introduction, the chalcogenide alloys have been widely studied for optical application since many years. Instead the material research for microelectronic application has just recently started. Although GST, in the most widely presented composition of $Ge_2Sb_2Te_5$, has demonstrated to be suitable as NVM for consumer application, still there is interest in the modification of some material properties to enable the use of PCM in other application. In particular increasing the retention temperature 10-years specification from the actual 85°C [16] exploring higher crystallization temperature alloys or reducing the set time below the actual hundreds of ns exploiting fast crystallization alloys. Obviously these two requirements are driving the development lines in different directions since the material properties that may fulfil both specification will not be the same (fast crystallization at high temperature for programming speed, slow crystallization at low medium temperature for retention).

The first attempt to work on material engineering has been driven towards the doping of the GST alloy, using nitrogen [8] or oxygen [17] in order to increase the crystal resistivity.

A more recent work has presented a deep characterization of the doped InGeTe (IGT) alloy [18] integrated into a PCM cell with the aim to improve the data retention required for industrial and automotive use. The study has shown that this chalcogenide features higher thermal stability (fig.2) and has demonstrated 10-years retention at temperatures above 150°C.

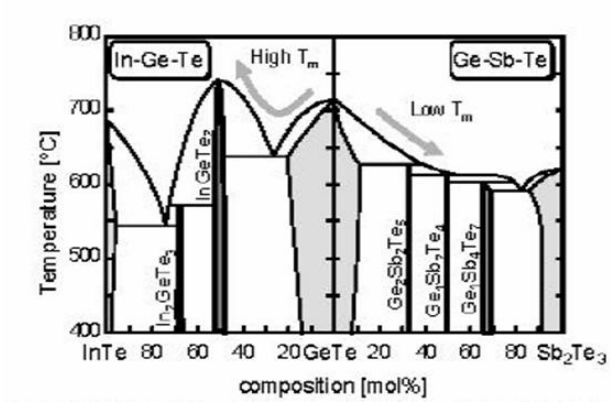


Fig.2: Pseudo-binary phase diagrams of GeTe-InTe and GeTe-$Sb_2Te_3$ systems [18].

Another solution with heterogeneous material based on composite Si-Sb-Te (SST) films has been investigated [19]. It has been reported that the writing current can be greatly reduced and much better data retention time can be obtained. The stronger thermal stability is attributed to the microscopic amorphous film nature, with nano-scale, locally-stabilized phase change clusters.

On the other side, in order to enlarge the PCM application there is a great interest to improve also the programming performances reducing the Set time, i.e. increasing the memory speed and in particular the overall programming throughput. Different research group have worked in this direction.

The doped GeSb is a material that combines fast crystallization speed with high crystallization temperature, thus offering the potential for fast but also non-volatile PCM [20]. It has been shown that the doped GeSb film has a crystallization temperature nearly 100°C higher than comparable thin film of undoped GST (fig.3), and exhibits only moderate changes in crystallization properties even at ultra-thin film thicknesses. Using an innovative PCM cell concept, that exploits the self-heating approach, it has been demonstrated that the doped GeSb phase-change material offers the potential for both fast crystallization and good data retention even at elevated temperature.

Another alloys considered to integrate PCM cell is based on doped SbTe [21]. The doped-SbTe material exhibits crystallization temperature at around 170°C, well higher than GST (fig.3). Also in this work it has been demonstrated that the fast-growth material doped-SbTe is suitable for use in PCM devices. Moreover the doped-SbTe material has shown low threshold field and symmetrical, short programming times (less than 30 ns for both Reset and Set operation), which definitely can be exploited to enhance the memory performances.

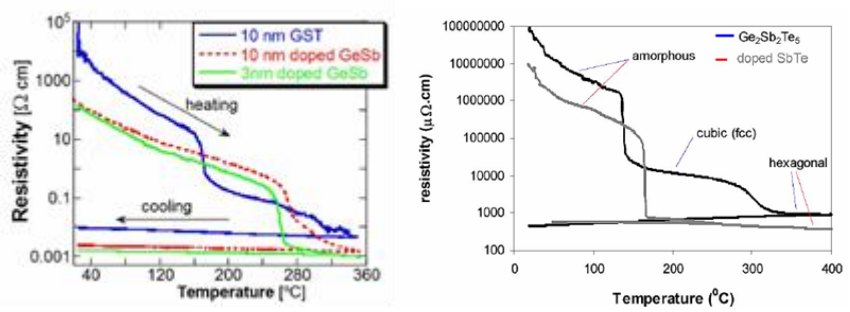


Fig.3: Comparison of the temperature dependent resistivity of as-deposited $Ge_2Sb_2Te_5$ (GST) and doped GeSb film (left side, [20]) and doped-SbTe film (right side, [21]).

**Summary** — The integration of the PCM concept, cell structure, array and product vehicle in a standard advanced CMOS technology has been widely assessed and demonstrated. The process integration results obtained so far and the level of comprehension of the PCM integration details allow moving the next development steps into the manufacturing and into the scalability validation of the PCM technology. The research of different alloys with respect the $Ge_2Sb_2Te_5$, today considered as the reference material for microelectronic application, will allow to enhance the performances of the PCM cell and to enlarge the spectrum of its applications.

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