Physics of electrical conduction in the sub-threshold regime and crystallization due to thermal disturbances in phase-change memory

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ABSTRACT

The physics of phase-change memory (PCM) cells is studied by investigating the scaling behavior of the off-state conduction with the amorphous region thickness and the crystallization time due to thermal disturbances. The trap spacing is extracted as one of the key parameters that affect the electrical conduction in the sub-threshold region by measuring both sub-threshold slope and activation energy based on the Poole-Frenkel model. It is found that the trap spacing can change while programming the PCM cell. The time for re-crystallization due to thermal disturbances, the other physical important aspect of the off-state PCM cell, is also studied for various amorphous volume fractions and different programming schemes. Controlling the pulse-tail duration may be preferable if one seeks for better retention properties at elevated annealing temperatures. The crystallization time is also found to be highly dependent on the resistance drift between thermal disturbances.

Key words: phase-change memory, trap spacing, activation energy, crystallization, resistance drift

1. INTRODUCTION

Phase change memory (PCM) has been extensively studied as one of the most promising candidates for the future memory technology due to its excellent endurance, long retention, fast speed, and scalability [1-4]. Despite significant research efforts on scaling the device dimension to achieve lower programming currents [5], a number of physical phenomena are still not very well understood. For example, the scaling behavior of the off-state conduction has not been made clear, which is of great importance for designing high performance PCM device and solving problems such as variability in threshold voltage and resistance drift. Another lack of sufficient physical understating is on crystallization properties of PCM cells. The recrystallization process, where a portion of the amorphous region formed by the RESET process goes back to the crystalline phase, allowing the current flow through the device and hence resulting in a low-resistance state, is highly dependent on the ambient temperature of the cell. This can be a serious issue when the temperature disturbance from the neighboring cells that are being programmed causes partial crystallization of the cell, resulting in retention failure [6].

The first part of this paper shows our novel method based on the trap-limited transport model (Poole-Frenkel model, PF model hereinafter) [7] to directly measure the key physical parameter, the inter-trap spacing (the spacing between the localized states) and investigate its dependence on the scaled amorphous layer thickness by using a novel phase change memory (PCM) cell structure with Additional Top Electrode (ATE). Simulations based on the PF model were also performed to validate the experimental data. The observed scaling behavior of the off-state conduction with amorphous layer thickness suggests that a more accurate analytical model for sub-threshold conduction especially at very small dimensions needs to be developed.

In the second part of this work, we develop an experimental methodology to investigate both the cell resistance and the drift dependences of the crystallization properties at shorter time scales (μsec) using an on-chip Micro-Thermal Stage (MTS). In order to allow the cell resistance to drift without thermal disturbances and thus separate drift from crystallization, we applied multiple short pulses to the MTS heater instead of monitoring the resistance change while being heated by a single long pulse as in [6]. Our results using a doped SbTe alloy as phase-change material [8] show

that the crystallization properties vary significantly with the nature of the amorphous region and depend on the drift properties of the cell as well.

2. EXPERIMENTS

The schematic comparison of the typical PCM cell with our proposed ATE device structure is shown in Fig. 1. The ATE layer confines the amorphous region to a well-defined thickness region (GST1) when the cell is programmed in the reset state. This is different from the typical PCM mushroom cell where the thickness of the amorphous region (u_a) is not well known during programming. This knowledge of exact thickness of u_a enables us to extract the trap spacing (Δz) directly by measuring the I-V characteristics of the PCM cell. The validity of the structure and the detailed fabrication process of the ATE device were described elsewhere [6]. Electrical measurements were performed using Agilent-4156C analyzer and Agilent-33250A waveform generator.

In order to study how the amorphous region crystallizes back to its crystalline counterpart by thermal disturbances, we use a structure called MTS that has a platinum (Pt) heater built on top of the lateral PCM cell (See Fig. 2 for the device structure). This enables the short time scale study which is comparable to the device operation (μsec). The measurement setup consists of two sets of electrical pulses applied to the device as shown in Fig. 3. One is the voltage pulse applied directly to the PCM cell to program the PCM cell to high-resistance (RESET) state initially and read the cell resistance afterwards during heating. Another pulse is the 100 μs-long heating pulse applied to the platinum heater (MTS). The heating pulse is applied as multiple short pulses or thermal disturbances separated by a time delay (t_p) that can be controlled.

3. RESULTS & DISCUSSION

3.1. Physics of sub-threshold conduction

We swept the DC current from 0 to 50 μA for the PCM cell in the RESET state to get the I–V curves of our proposed ATE device, which is programmed with various RESET voltages of 1.4, 1.5, 1.6, and 1.7 V. The ATE device is considered to be fully programmed (i.e., GST1 layer is completely amorphized) when the threshold voltage remains saturated for increasing reset voltages as seen in the figure. In this case the RESET voltage for the fully amorphized GST1 layer is observed to be around 1.6 V. According to the trap-limited transport model, the conduction in the amorphous state is due to the hopping of the electrons from one trap to another assisted by the electric field, commonly referred as Poole-Frenkel (PF) mechanism. When a voltage is applied, the potential barrier for the carriers is reduced in the direction parallel to the electric field and the current gets increased as depicted in Fig. 5.

Based on this analytical PF model, both sub-threshold slope (STS) and activation energy (E_A) for conduction depend linearly on the normalized trap spacing with respect to the amorphous region thickness ($\Delta z/u_a$) [7]. This provides a straightforward procedure for estimating the average inter-trap distance, once the amorphous thickness is known for the ATE devices. Fig. 6 shows the sub-threshold I-V characteristics for the fully programmed ATE devices of different thicknesses. It is seen from the figure that STS is a strong function of amorphous thickness, and our experimental data (symbols) are confirmed by simulation (lines) based on the PF model. By using the PF model and applying it to fit our experimental data with Δz as a fitting parameter, we could extract the trap spacing Δz and find that the trap spacing significantly changes for different amorphous thicknesses (~ 5 nm to ~ 7 nm for amorphous thickness of 8 nm to 30 nm, respectively).

The next three figures (Fig. 7 - Fig. 9) provide another methodology to measure the trap spacing Δz by activation energy measurements. Since activation energy for conduction is also a linear function of the relative ratio of trap spacing to amorphous thickness as in sub-threshold slope, we should be able to measure the trap spacing if we measure the activation energy as a function of applied bias voltage given the amorphous thickness. We therefore measured I-V characteristics for the amorphous chalcogenide whose thickness is 8 nm at elevated temperatures of 30, 40, 50, and 60 °C in Fig. 7. Current increases obviously as temperature increases due to the relatively large activation energy E_A of electron hopping in chalcogenide glasses.

We next show the Arrhenius plot of the measured current at different voltage bias values in Fig. 8. It is found that the extracted activation energy decreases correspondingly to the increased applied bias voltage, which is consistent with the trap-limited transport model [7]. As shown in Fig. 9, we finally extracted the trap spacing values for different amorphous thicknesses (8nm, 20nm, and 30nm) from the slope of activation energy vs. applied bias voltage plot. Fig. 10 summarizes the trap spacing values used to fit the I-V curve in the sub-threshold regime and compare the values extracted from the two different experimental methods (STS and E_A). It can be seen that the average trap spacing increases linearly with the amorphous thickness in contrast to the general assumption that the trap spacing remains constant for different thicknesses [7].

3.2. Physics of recrystallization

Fig. 11 shows the typical crystallization curve for a PCM cell with its own local MTS heater at the annealing temperature (T_A) of about 270 °C. With the heating pulse of 100 μs width and 1 μs rising/falling time turned on, the resistance gradually decreases until the crystallization path begins to be formed. As can be seen in the inset, the PCM cell is electrically programmed with RESET/SET resistance ratio of ~ 1000 and at least 100 cycles of SET and RESET programming are performed before each measurement of the crystallization time (t_{crys}) to verify that the PCM cell characteristics are stable at both SET and RESET resistance values. By finding the number of annealing pulses required to fully crystallize the PCM cell in Fig. 11, the crystallization time is found to be about 4 ms for the annealing temperature of 270 °C with V_{Pt} of about 6 V.

To see the dependence of the crystallization time on the initial cell resistance, the PCM cells were programmed to different resistances and the crystallization times were measured for various temperatures in Fig. 12a). As seen in the figure, the crystallization time exponentially decreases with the increasing temperature following the Arrhenius equation [9]. The activation energy for crystallization [10] is extracted from the slope of the t_{crys} versus $1/kT_A$ (k is the Boltzmann constant) plot in Fig. 12a), and it is found to be about 2 eV. It should be noted that further increase of the cell resistance toward the full-RESET value of about 6M Ω results in almost the same crystallization time. This trend of an initial increase of crystallization time with increasing cell resistance and saturation afterwards is more clearly observed in Fig. 12b) which shows the crystallization times as a function of cell resistances, R.

We next investigate the difference in crystallization behavior for three different programming schemes used in multi-level applications. In the first scheme, the various intermediate resistances are obtained by applying the reset pulses of different amplitudes (Pulse-Amplitude Control, PAC). In the second scheme, a reset pulse with a maximum reset amplitude is applied to the cell and the fall time of this pulse is controlled to vary the quenching time of the molten phase-change material within the cell [11] (Pulse-Tail Duration Control, PDC). In the last scheme, we control the filament formation during the SET process [12] by applying SET pulses of varying amplitudes (Current-Filament Control, CFC) to the cell which is initially programmed to the full-RESET state. For each intermediate resistance state, the cell is subjected to consecutive thermal disturbance pulses causing a temperature rise of about 220 °C. It can be seen in Fig. 13 that for the cells with the same resistance state, the crystallization time is much smaller for the current filament control case than the other schemes. This can be explained by a growth-dominated mechanism of the crystallization starting from the already-present crystalline filament boundaries in these intermediate states [12].

Lastly, we study the dependence of the crystallization time on the resistance drift in Fig. 14 with the PCM cells programmed to the same initial amorphous resistances. The effect of drift is incorporated by changing the time interval (t_p) between the consecutive heating pulses applied during the crystallization process. This difference in time intervals between the two pulses will cause the cells to drift differently, as the resistance drift is related to time by a power-law equation [13]. It is clearly seen in the figure that the crystallization occurs faster as we decrease the time interval from 10 s to 1.2 s. Fig. 14 also shows that the statistical variation which arises from the random nature of the crystallization process is found to be quite large, so more than 10 samples of crystallization time measurements have been averaged for each time interval to give statistically reasonable values with 1-sigma (σ) uncertainties. Since the drift of the RESET resistance follows the phenomenological power law with time, it is concluded from the above results that the resistance drift can decelerate the crystallization process. It is noted from this finding that if a PCM cell is RESET-programmed, it would be better to program the neighboring cells at a later time, allowing the current cell to drift for some time. This would lower the probability of cell failure due to thermal disturbances.

4. CONCLUSION

The linear dependence of the trap spacing on the dimension of amorphous state region is presented by using a novel PCM structure with ATE. We have found that the trap spacing value ranges from 5 nm to 8 nm for the amorphous thicknesses of less than 30 nm. This finding will help to develop an accurate model to describe the scaling behavior of the conduction and switching characteristics in PCM and to design the ultra-thin film based PCM devices. We also investigated how the amorphous state is affected by thermal disturbances in such aspects as different annealing temperatures, cell resistances, and programming schemes for multi-level PCM cells. The re-crystallization time is found to be significantly dependent on the resistance drift between thermal disturbances.

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Biographies

Chiyui (Ethan) Ahn received his B.S. degree and M.S. degree (in Electrical Engineering) from the Korea Advanced Institute of Science and Technology (KAIST) in 2005 and 2007 respectively. During his Master's years, he simulated various nanoelectronic devices such as Nanowire/Carbon Nanotube FETs and Schottky-Barrier Tunnel Transistors. He joined the Korea Institute of Science and Technology (KIST) in 2007. While at KIST as a research scientist, he worked on fabrication of Spin-Transfer-Torque MRAM (STT-MRAM) devices with e-beam lithography technology. In September 2010, he joined Stanford University as a Ph.D. candidate in Electrical Engineering and doing an extensive research on the future non-volatile memory under the supervision of Prof. Philip Wong. His research interests are in nanoscale electronic devices, especially phase-change memories (PCM) and resistive switching memories (ReRAM).

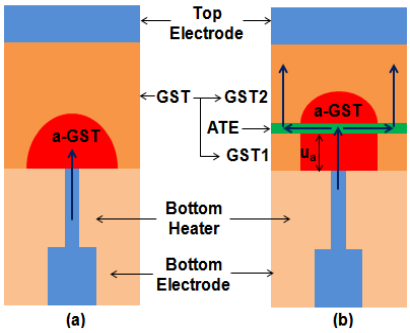

Fig. 1. (a) A typical T-shape PCM cell and (b) a pseudo 3-terminal device with an ATE layer where the amorphous region of well-defined thickness is confined between the ATE and heater.

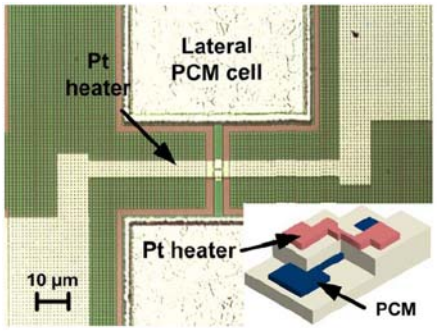

Fig. 2. Top view microscope image of a lateral PCM cell with a micro-thermal stage (MTS) heater. The inset shows the 3D bird's eye view.

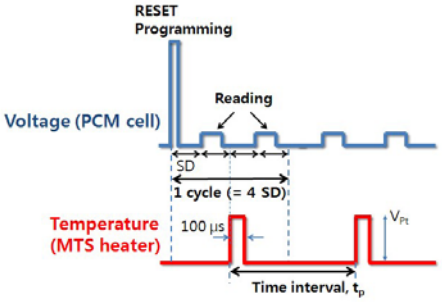

Fig. 3. Electrical pulse profiles for RESET-programming, reading (blue pulses), and MTS heating (red pulses). Reading voltage is set at V_{READ} ~ 0.1 V.

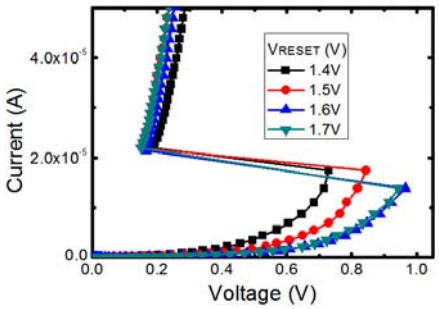

Fig. 4. RESET state current-sweep I–V curves of the ATE device programmed with various RESET voltages (V_{RESET}), showing that the fully RESET voltage is 1.6 V.

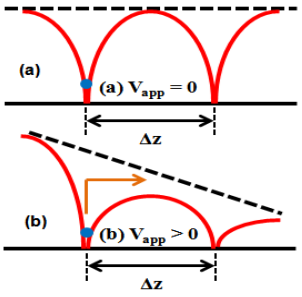

Fig. 5. (a) Schematic that shows the electron trapped in the localized states and the inter-trap spacing is Δz. (b) The application of a voltage (Vapp) lowers potential barrier, enhancing transport.

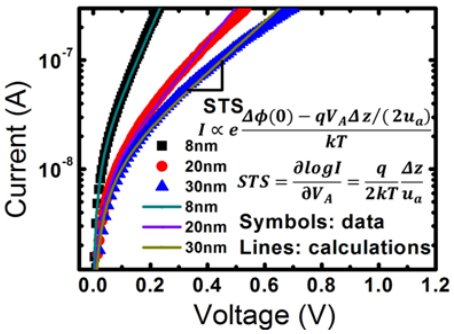

Fig. 6. Sub-threshold I-V characteristics for fully programmed ATE devices with different amorphous thicknesses. The equation shows its linear dependence on $\Delta z/u_a$.

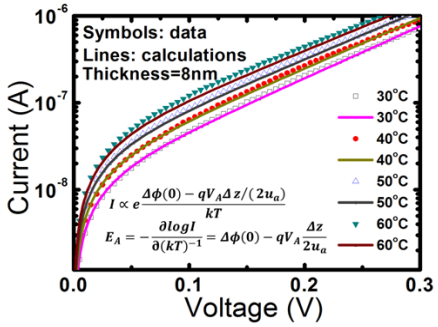

Fig. 7. Measured I−V characteristics for the ATE devices at different temperatures, with simulated curves also shown in the figure.

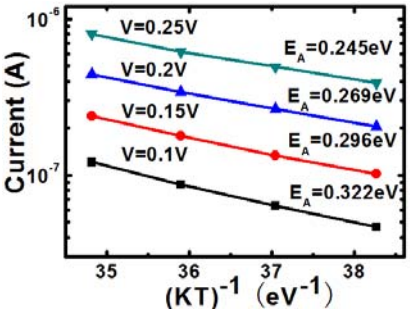

Fig. 8. The Arrhenius plot of the current measured at four different voltages. The extracted activation energy decreases for increasing voltages.

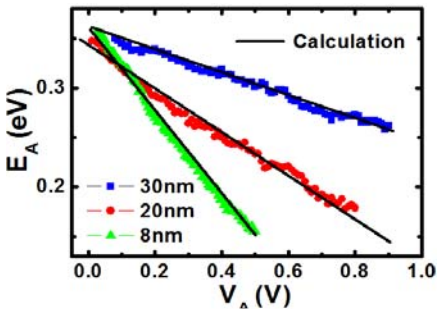

Fig. 9. Activation energy E_A of sub-threshold current as a function of applied voltage V_A for different amorphous thicknesses.

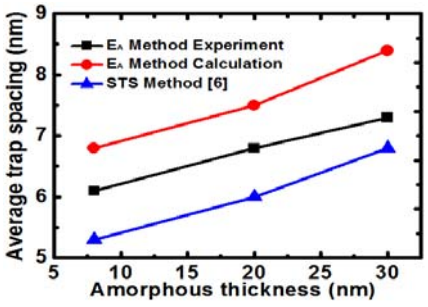

Fig. 10. Average trap spacing values for the different amorphous thicknesses of ATE devices. Trap spacing scales with amorphous thickness.

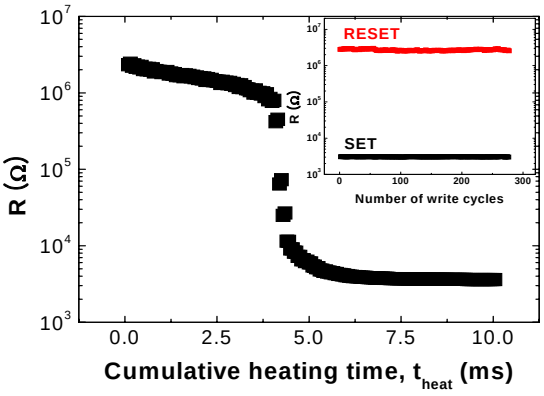

Fig. 11. Crystallization by MTS heating at T_A ~ 270 °C. The crystallization time (t_{crys}) is extracted to be the cumulative heating time needed to form the first crystallization path within the amorphous region in the PCM cell. The inset shows the endurance characteristics with a high RESET/SET resistance ratio of ~ 1000.

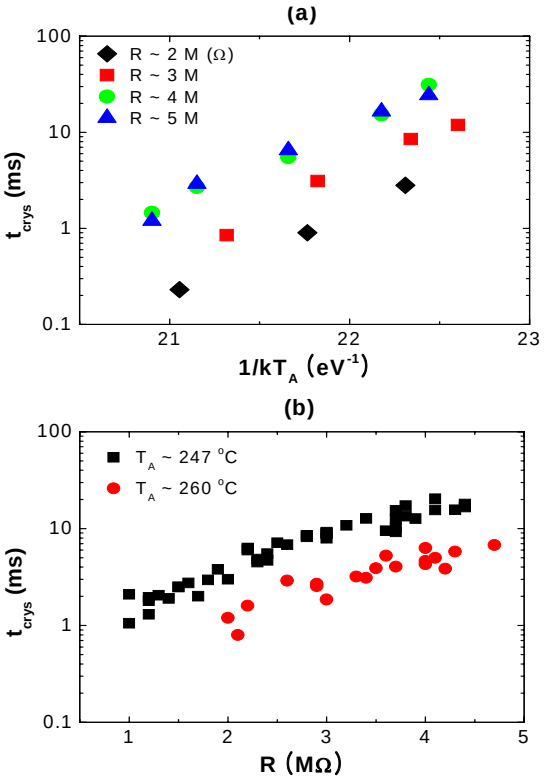

Fig. 12. (a) Temperature (T_A) dependence of the crystallization behavior for different cell resistances of 2, 3, 4, and 5 M Ω and (b) cell resistance (R) dependence for two different temperatures. PCM cells are initially programmed to different resistances by the RESET pulse of different voltage amplitudes.

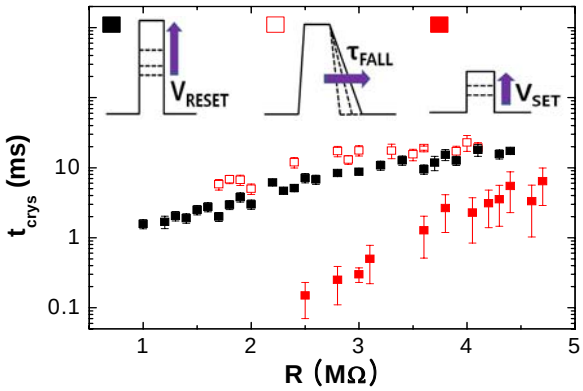

Fig. 13. Crystallization times for the PCM cells in the intermediate states by different programming schemes. Programming scheme 1 (black solid square) is to control the pulse-amplitude starting from the full-set state, scheme 2 (empty red square) modulates the pulse-tail duration starting from the full-reset state, and scheme 3 (solid red square) represents the current-filament control. T_A is maintained at 247 °C.

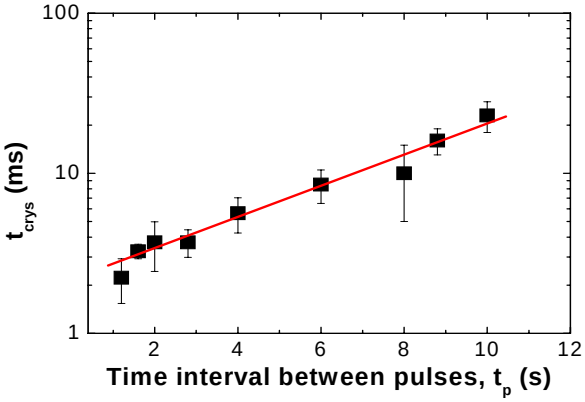

Fig. 14. The crystallization time (t_{crys}) versus time interval between pulses (t_p). The error bar shows the statistical variations (1-σ) from repetitive measurements of the crystallization time, and the linear fit line is drawn to show that it lies within the uncertainties.