Demonstration of a High-Speed Multi-Level Cell Phase-Change Memory Using Ge-doped SbTe

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ABSTRACT

We demonstrate a high-speed multi-level cell (MLC) operation of a phase change memory with a Ge-doped SbTe (Ge-ST) for the first time using a conventional pore-type device structure as well as a conventional programming method. The Ge-ST was selected to have a low Sb/Te ratio of 1.6 (Ge-ST_L) rendering a diminished growth speed and a nucleation time relative to the case of a high Sb/Te ratio typical of fast growth-dominated crystallization. With a writing time of less than 100 ns, each of the 4 resistance levels separated from one another at least by the factor of 4 is shown to form reliably and stay with a low drift coefficient ranging 0.067 - 0.1. Ge-ST_L may thus be regarded as a promising material for high-speed MLC phase change memory applications.

Key words: *Ge-doped SbTe, Multi-level cell, Phase change memory*.

1. INTRODUCTION

Phase change memory (PCM) is a promising candidate for the next generation non-volatile memory applications, and multi-level cell (MLC) technique is potentially important to enhance the data storage density of PCM. The MLC technique employs a write-and-verify (WAV) scheme to ensure the formation of multiple resistance levels sufficiently near the respective targeted levels. As a rule, repetitive WAV cycles are needed to write a single data bit properly and this is time-consuming. For example, T. Nirschl *et al.* reported that it took about 1 μs to complete a WAV cycle for the $Ge_2Sb_2Te_5$ (GST)-based PCM using a modulated-current (MC) method for write, and 6 - 12 WAV cycles *viz.* about 10 μs were needed to store one data bit for more than 60% of the PCM cells [1]. Obviously, a PCM of a faster write speed is required to speed up a WAV cycle. In this regard, PCM with Ge-ST is attractive due to its much faster write speed by about one order than that of the GST-based PCM [2]. Ge-ST's having high Sb/Te ratios are known to display very rapid growth-dominated crystallization which tends to make the MLC operation with the existing programming methods practically unfeasible, seemingly accountable for the lack of demonstration of the sort to date. In our earlier study using Ge-ST's of varying Sb/Te ratio from 1.9 to 4.2, it was shown that growth speed diminished with decreasing Sb/Te ratio over the whole range and nucleation time decreased rapidly as well in the range of Sb/Te ratio from about 2.6 downward [3]. In this study, we selected the Ge-ST of a low Sb/Te ratio of 1.6 (Ge-ST_L) with the aim of exploiting both factors potentially to form and control multiple resistance levels reliably. With the conventional pore-type PCM devices and the MC method, we demonstrate a high-speed 4-level cell operation for the Ge-ST_L PCM.

2. EXPERIMENTS

The Ge-ST_L PCMs were fabricated following the essentially same procedure as in our early studies [2,3]. A device was made to have a 300-nm-thick TiN/Ti bottom electrode, a 300-nm-thick Ge-ST_L active layer co-sputtered from a Ge and a SbTe targets to fill a 150×150 nm^2 contact pore, and a ~300-nm-thick TiN/Al top electrode. The setup for electrical characterization of the Ge-ST_L PCMs is referred to in ref. [2]. The load resistance was 1kΩ in this study.

3. RESULTS & DISCUSSIONS

A Ge-ST_L PCM was found to have the typical current-voltage (I-V) curve of Fig 1 showing the threshold switching voltage of about 0.85V. The current-resistance (I-R) characteristics of a Ge-ST_L PCM are shown in Fig. 2. With the trailing edge of the programming pulse increasing from 5 ns to 20 ns, transition from SET to RESET states progresses more gradually with current, providing the margin for MLC operation. Specifically, a SET state was formed to have

the resistance of $10^3\,\Omega$ (corresponding to D0 data state) with a current pulse having the waveform of 5/60/5 ns and the amplitude of 2.0 mA. The other resistance levels of the PCM were about $10^4\,\Omega$, $10^5\,\Omega$, and $6\times10^5\,\Omega$ (corresponding to D1, D2 and D3 data states respectively), formed by current pulses of the waveform of 5/60/20 ns and amplitudes of 2.8 mA, 3.1 mA, and 3.5 mA, respectively. These four resistance levels, with adjacent levels being separated by the factor of 4 at least, were maintained clearly throughout 10^3 writing cycles tested as shown in Fig. 3. A cumulative distribution of the resistance levels for 20 Ge-ST_L PCM cells operated with the respective writing parameters at best guess[1] is shown in Fig. 4. A WAV scheme can be applied to improve the level clearance in Fig. 3 and Fig. 4 for practical MLC application [1]. Moreover, these levels were found to display low drift coefficients of ~0.067-0.1 as shown in Fig. 5, maintaining the level clearances well for more than 10^3 s at 300°K as shown in Fig. 6.

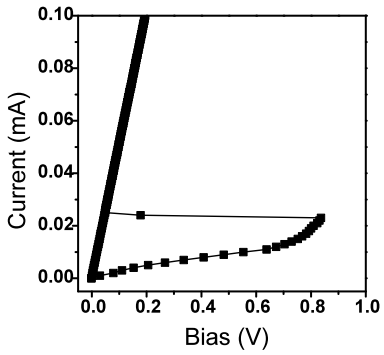

Fig. 1. I-V characteristics of the Ge-ST_L PCM

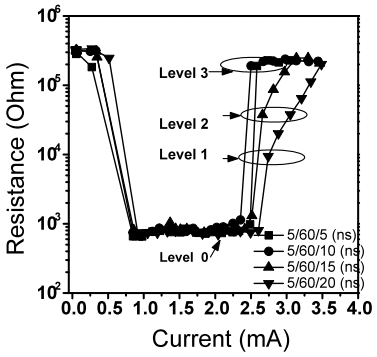

Fig. 2. I-R characteristics of the Ge-ST_L PCM

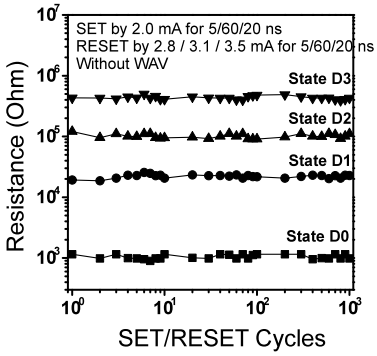

Fig. 3. The cyclability of the Ge-ST_L MLC PCM

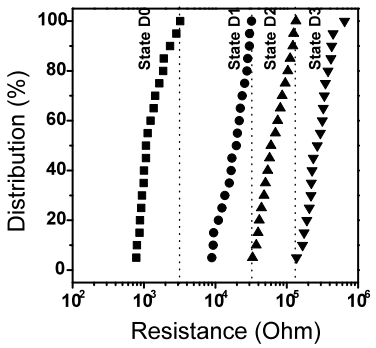

Fig. 4. Cumulative distribution of the resistance levels for 20 Ge-ST_L PCM cells

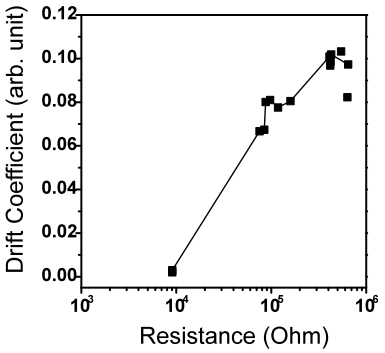

Fig. 5. The drift coefficients of the Ge-ST_L PCM at various resistance levels

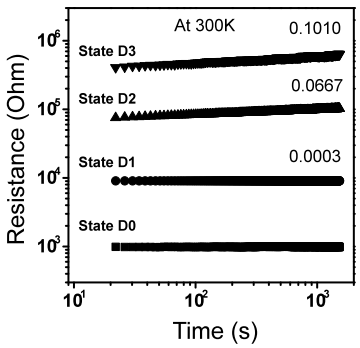

Fig. 6. The resistance-level drift characteristics of the Ge-ST_L PCM in room temperature.

4. CONCLUSION

A Ge-ST_L MLC PCM is demonstrated using a pore-type device structure and the conventional MLC operating method to suggest that Ge-ST_L may be a promising material for the high-speed MLC PCM applications.

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