A Novel Cell Technology for Phase Change RAM

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Abstract

We have integrated a phase change random access memory (PRAM), completely based on 0.24μm-CMOS technologies using nitrogen doped GeSbTe films. The $Ge_2Sb_2Te_5$ (GST) thin films are well known to play a critical role in writing current of PRAM. Through device simulation, we found that high-resistive GST is indispensable to minimize the writing current of PRAM. For the first time, we found the resistivity of GST film can be controlled with nitrogen doping. Doping nitrogen to GST film successfully reduced writing current. A 0.24μm PRAM using N-doped GST films were demonstrated with writing pulse of 0.8mA-50ns for RESET and 0.4mA-100ns for SET. Also, the cell endurance has been enhanced with grain growth suppression effect of dopant nitrogen. Endurance performance of fully integrated PRAM using N-doped GST shows no fail bit up to 2E9 cycles. Allowing 1% failures, extrapolation to 85°C indicates retention time of 2years. All the results show that PRAM is one of the most promising candidates in the memory market for the next generation memories.

Keywords: Phase Change RAM, GeSbTe, N-doped , CMOS, Memory

1. Introduction

There are growing needs for a nonvolatile memory technology for high density stand alone as well as embedded complementary metal oxide semiconductor (CMOS) applications with faster speed and higher endurance than conventional nonvolatile memories. PRAM is a promising device to meet these needs of market. A phase-change memory array based on chalcogenide materials was first reported in 1970s [1][2][3]. Improvements in phase-change material technology subsequently paved the way for development of commercially available compact disk rewriteable (CD-RW) and digital versatile disk (DVD) optical memory disks [4]. These advances, coupled with significant technology scaling and better understanding of the fundamental electrical device operation, have motivated development of the PRAM technology at the present technology node[5]. As portable application market rapidly expands, commercialized memories like Flash memory, dynamic random access memory (DRAM) hardly satisfy various needs such as non-volatility, low power, high density, and low cost. The volatile memories like DRAM and static random access memory (SRAM) are commonly used in the personal computers, which are fast and have good endurance property. Instead, Flash memory which is widely used in the portable applications, is non-volatile. However it has problems in writing speed and endurance. Therefore, high speed, good endurance, non-volatile memories are attractive and several candidates like ferroelectric random access memory (FeRAM), magnetic random access memory (MRAM), PRAM are actively studied. Compared with the novel non-volatile memories (such as FeRAM, MRAM, PRAM), Flash memory has advantages in the memory density and production cost, but the basic performance in writing speed and endurance is not enough. MRAM, FeRAM have the advantages in speed, power and endurance, but have disadvantages in the density and the cost. PRAM is 1000 times faster than Flash memory and even cheaper in production cost because of its simple structure. However, PRAM has a demerit in scaling due to high writing current (>1mA) through a large switching transistor(TR). Cell area is determined by the size of CMOS transistor[6]. In this paper, a novel solution for the low current operation of PRAM will be presented.

2. Device Integration

The transmission electron microscope (TEM) image in figure 1 shows the fully integrated PRAM. Three metal layers are used in PRAM . The GST cell is placed between Metal 0 and Metal 1 layers connecting the bottom electrode contact (BEC) to the top electrode contact (TEC). CVD TiN is filling the BEC compactly and the interface between the BEC and GST is smooth.

3. Results and Discussion

PRAM uses a short high current pulse to make the amorphous state (high resistance RESET state), and low but a bit longer current pulse to get the polycrystalline state (low resistance SET state) as shown in figure 2. During the amorphizing RESET pulse, the temperature of the programmed volume of phase-change material exceeds the melting point which eliminates the polycrystalline ordering in the material. When the RESET pulse is given, the device quenches to "freeze in" the disordered structural state. This quenching time (falling time ~few ns) is determined by both the thermal environment of the device and the fall time of the pulse. The crystallizing SET pulse is of lower amplitude and of sufficient duration (crystallization time~100ns) to maintain device temperature in the rapid crystallization range for a sufficient time for crystal growth. Figure 3 shows I-V curves of SET/ RESET state of fabricated PRAM. At low reading voltage, the device exhibits either a low resistance (~1KΩ) or high resistance(>100KΩ), depending on its programmed state. To program the device, a pulse of sufficient voltage is applied to drive the device into a highly conductive state (dynamic on state). For a RESET device, a voltage higher than threshold voltage (Vth) is required. Vth is a device design parameter and is chosen to be around 1.1V for current memory applications. To avoid reading disturbance, the device read region is well below Vth and also below the reset regime. The device is programmed while it is in the dynamic on state. The final programmed state of the device is determined by the current amplitude and its duration time in the dynamic on state.

PRAM using undoped GST films can be operated with 1.8mA-50ns RESET current and 1.2mA to 1.5mA-100ns SET current. This RESET current is too high for reasonable CMOS transistor size. Figure 4 shows the simulation results of the temperature distribution in the GST cells with different resistivity (a) 2mΩ-cm (undoped GST) and (b) 20mΩ-cm (high resistive GST. 1mA-50ns RESET current pulse was applied to the cells with BEC size of 80nm. After GST deposition, GST is crystallized due to the thermal budget of 400 ^{o}C during the metal contact formation, which reduces its resistivity down to 2 mΩ-cm. In this case, the corresponding temperature distribution in Figure 4(a) displays 141 ^{o}C maximum at the BEC-GST contact, which is not high enough to melt GST. On the other hand, Figure 4(b) for high resistive GST (20mΩ-cm) shows that the temperature increases to 973°C, which is high enough to melt GST. Therefore, it is very important to optimize the resistivity of GST film for low power operation of PRAM.

For the first time, we found the resistivity of GST film can be controlled with nitrogen doping. The nitrogen concentration of N-doped GST films in the range of 0-10at% were obtained by varying the nitrogen gas flow rate in the range of 0-10sccm, and the argon gas flow rate was fixed at 100sccm[7]. Figure 5 shows that the resistivity of GST film increases sensitively with nitrogen concentration. The resistivity was controllable in wide range from 7 mΩ-cm to 500 mΩ-cm. Indeed, Figure 6 shows the resistivity of undoped GST and N-doped GST (N=7at%) films as a function of annealing temperature range between 150°C and 400°C. The resistivity of undoped GST and N-doped GST (N=7at%) films decreased with annealing temperature. The resistivity of N-doped GST (N=7at%) film is measured to be as high as 20 mΩ-cm after 400°C annealing while that of undoped GST film decreases below 2mΩ-cm. Figure 7 shows X-ray diffraction (XRD) result before and after anneal for undoped GST and N-doped GST (N=7at%) films. Figure 7(a) shows XRD spectrum for undoped GST film obtained from an as-deposited which was identified as a NaCl-type structure (FCC). After annealing at 400°C, XRD spectrum of undoped GST film was changed a hexagonal structure (HCP)[8]. Figure 7(b) shows XRD spectrum for N-doped GST film obtained from an as-deposited and annealed at temperature of 400 °C which were identified as a NaCl-type structure. The XRD results show N-doped GST films were thermally more stable than undoped GST film.

Figure 8 shows TEM micrographs of undoped GST and N-doped GST films after 500°C annealing. From

TEM micrographs, the grain size of undoped GST film has larger than 100nm. The grain size of N-doped GST film has about 30nm. We can see that N-doped GST has smaller grains than undoped GST film because nitrogen suppresses the GST grain growth when heated. At N-doped (N=7at%) GST film small grain makes resistivity as high as about 20mΩ-cm and increases crystallization temperature by 45°C enhancing thermal stability[7].

N-doped GST based PRAM can be operated with 0.8mA-50ns RESET current and 0.4mA-100ns SET current. Especially, RESET current is remarkably reduced compared to the undoped GST case of 1.5mA.

Reliability is another critical requirement for PRAM in order to be a future commercial memory. Figure 9 shows the I-V characteristics of undoped and N-doped PRAM cell before and after 2E7 cycle test. Although the cell using undoped GST is degraded after cycling, the cell using N-doped GST is excellent IV characteristics after cycling because of the enhancement of thermal stability of RESET(amorphous) state. Also the RESET/SET ratio of resistance remains higher than 10 after 2E7 cycle test for N-doped GST, while that for undoped GST becomes as low as 2 due to thermal unstability of undoped GST. Figure 10 shows cycling performance of fully integrated PRAM using N-doped GST. Endurance test shows no fail bit up to 2E9 cycles. During the test, one fail bit is occasionally observed, which originates from incomplete phase transition leading to small RESET/SET ratio. However, no fail is observed up to 2E9 cycles of reversible phase transition. Finally, the data retention time is estimated by reading the stored data after baking at 125, 150 and 175°C during 1, 10 and 100houres. Figure 11 shows data retention measurement at three temperatures. The data shows fail bit of the investigated chips at each temperature and each baking time. Allowing 1% failures, extrapolation to 85°C indicates retention time of 2years. Although the activation energy of amorphous GST increased with the doping of nitrogen to the GST film[7], the retention time on N-doped GST is shorter than that of previous work using undoped GST[5]. Optimization of PRAM cell structure and phase change materials is underway for improvement in retention time.

4. Conclusions

We have integrated a PRAM, completely based on 0.24μm-CMOS technologies. Writing current of PRAM is successfully decreased by doping nitrogen to GST and scaling BEC down to 80nm. A 0.24μm PRAM using N-doped GST was demonstrated with writing pulse of 0.8mA-50ns for RESET and 0.4mA-100ns for SET. We also notice that the endurance has been enhanced with grain growth suppression effect of dopant nitrogen. Endurance performance of fully integrated PRAM using N-doped GST films shows no fail bit up to 2E9 cycles. Allowing 1% failures, extrapolation to 85°C indicates retention time of 2years. PRAM is 1000 times faster than Flash memory and even cheaper in production cost, so PRAM is a promising device to meet needs of market.

References

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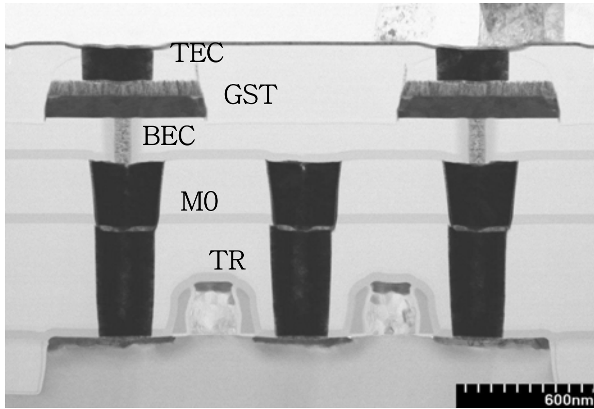

Fig. 1 TEM micrographs of the fully integrated PRAM.

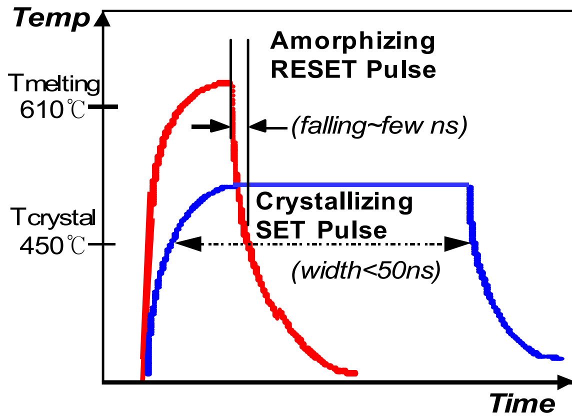

Fig. 2 Illustration of the time (pulse width) to temperature relationship of the phase change.

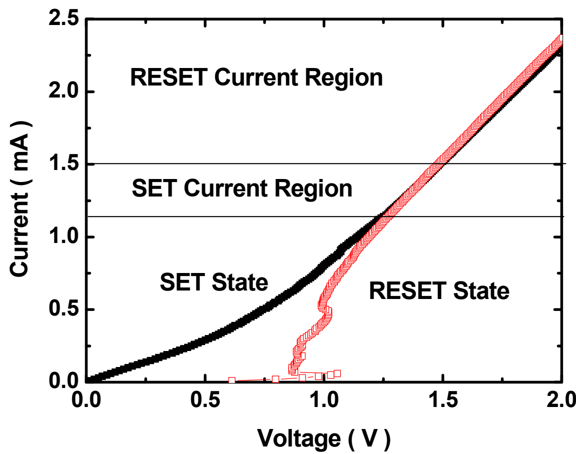

Fig. 3 I-V curves of SET/RESET state of fabricated PRAM

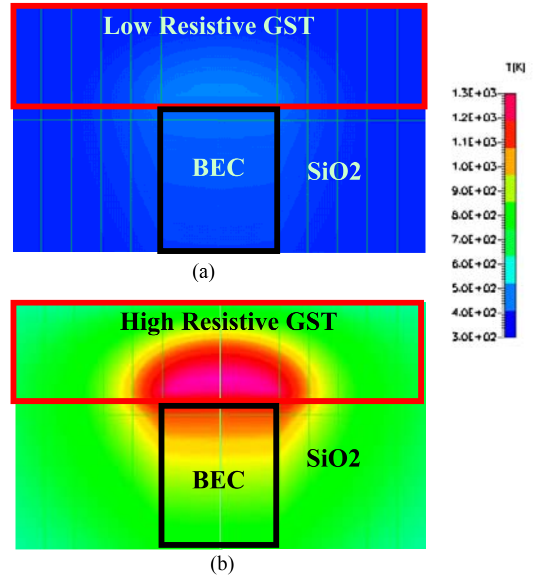

Fig. 4 Simulation result of cell temperature when the same RESET (1mA, 50ns) pulses are applied to two GST cells with different resistivity (a) 2mΩ-cm and (b) 20mΩ-cm.

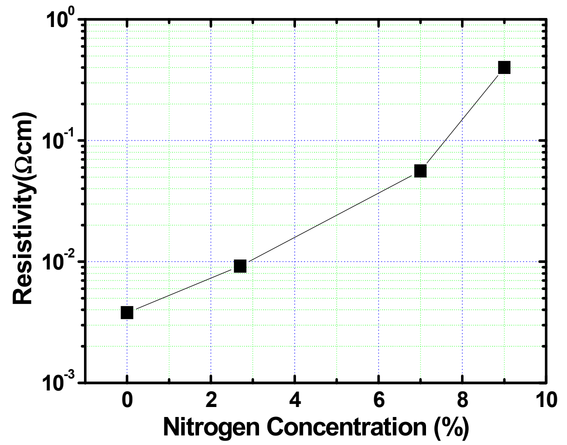

Fig. 5 Resistivity of the GST films as a function of nitrogen concentration.

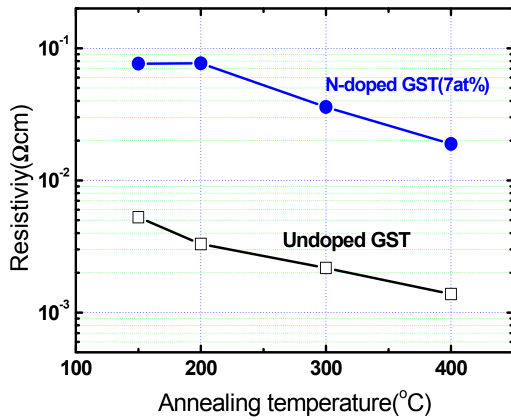

Fig. 6 Resistivity of the (a) undoped GST and (b) N-doped GST films as a function of annealing temperature.

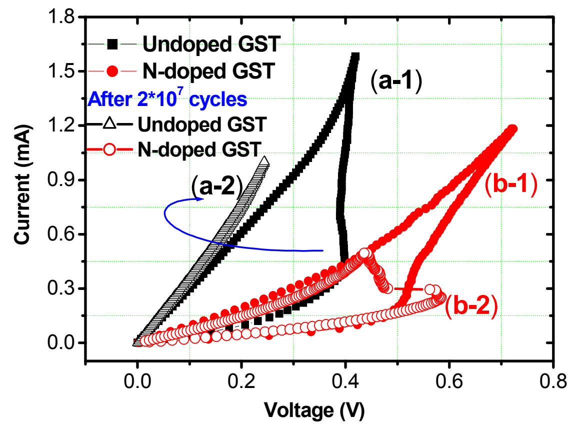

Fig. 9 I-V characteristics of the PRAM cell before and after 2E7 cycles : (a-1) undoped GST before cycles, (a-2) undoped GST after 2E7 cycles, (b-1) N-doped GST before cycles and (b-2) N-doped GST after 2E7 cycles.

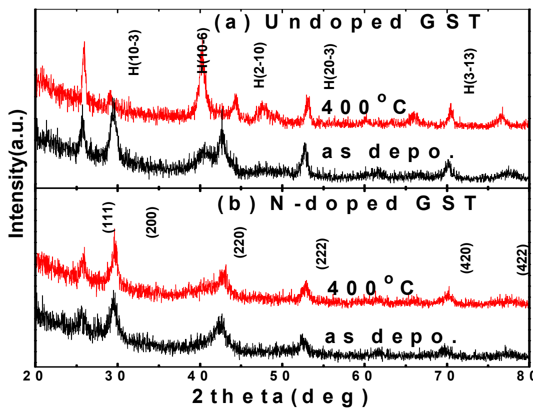

Fig. 7 XRD results before and after anneal for (a) undoped GST and (b) N-doped GST.

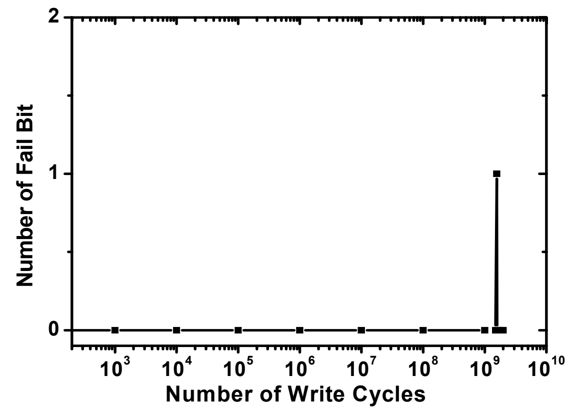

Fig. 10 Cycling performance of fully integrated PRAM using N-doped GST.

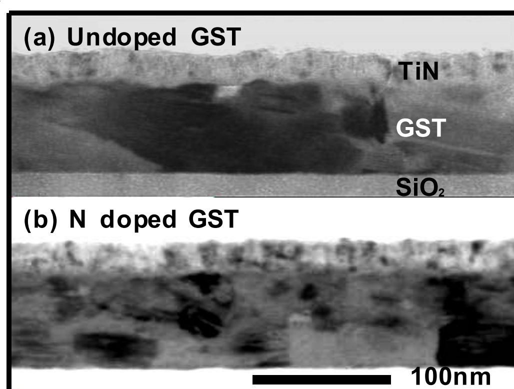

Fig. 8 TEM micrographs of (a) undoped GST and (b) N-doped GST films after 500°C annealing.

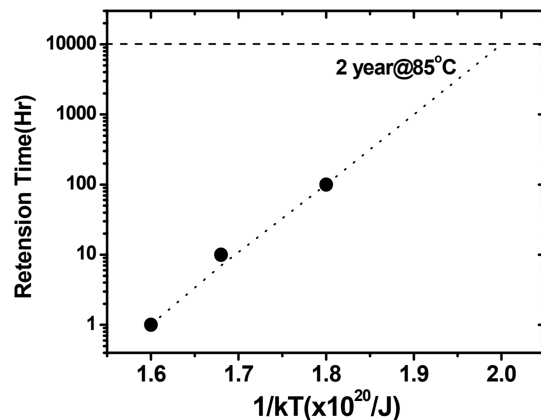

Fig. 11 Data retention measurement of fully integrated PRAM using N-doped GST.