

Phase change materials strategies for reset current reduction.

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ABSTRACT

In this paper, we highlight different strategies allowing reducing the reset current of Phase Change Memory (PCM) devices. First, we present the effect of the introduction of thin interfacial oxide layers in the structure and we show that large reset current reductions are achieved thanks to the reduction of the effective contact area dimension. [1] We then illustrate the effect of new elements additions into the phase change material matrix, and we demonstrate that significant reset current reductions can be obtained for quite low additives percentages. The example of the addition of Carbon into $\text{Ge}_2\text{Sb}_2\text{Te}_5$ is presented, [2] allowing us to point out the physical characteristics of the chalcogenide material at the origin of the reset current reduction. Finally, we present the effect of variations of the stoichiometry of the GeTe phase change matrix, [3] and in this case we illustrate the crucial role of the crystallization dynamics in the reset current reduction.

Key words: Phase Change Memories, Reset current reduction, Phase Change Materials

1. INTRODUCTION

Phase Change Memories (PCM) are one of the most promising concepts for the future generations of Non Volatile Memories for both stand-alone and embedded applications. Main advantages are the low programming voltages, fast read/write times, good scalability and low cost, due to the reduced number of fabrication masks compared to standard Flash memories. Technological developments have today enabled the advent of the first industrial products. Meanwhile, extensive work is performed on the Phase Change (PC) materials itself, aiming at the optimization of the cell properties for specific applications. In particular, for the embedded memory market, new materials developments target an enhancement of the PCM high temperature retention which is necessary for automotive applications, while a reduction of the writing current is desirable for consumer applications.

The reduction of the programming current is actually one of the main research axes in the field of PCM memories, first because of the limited current drive capability of the access device. Since the current provided by the access device scales with the size of the device, reducing the programming current is a critical issue to enable a high memory density and hereafter a low cost per megabyte. [4] Secondly, the high programming current of the PCM devices results in a relatively low programming bandwidth. In fact, while the programming time of a PCM cell is of the order of nanoseconds and about three orders of magnitude lower than for Flash, almost all the advantage is lost at the array level, where PCM and Flash both features programming bandwidths in the order of about 10 Megabits per second. [5] Consequently, a reduction of the programming current would greatly boost PCM performances.

In the case of a PCM device, a low programming current corresponds to a low reset current I_{rst} , since during a programming sequence, the current happens to be maximum during the reset operation which correspond to the amorphization of the PC material. During the reset operation, a volume of the PCM layer located in the highest current density region is heated above the melting temperature by Joule heating. When the reset current is switched off, this area is rapidly quenched down, so that a portion of the melted volume ends up in the amorphous state which is the high resistance state.

In this paper, we first review the different strategies available for reducing the reset current of analytical PCM cells and this will give us the opportunity to point out the physical parameters that are likely to impact the reset current I_{rst} . We then present different examples of reset current reduction resulting from PC materials modifications, like the introduction of thin interfacial oxide layers, the addition of new elements in the PC material or the modification of the stoichiometry of the PC material itself.

2. RESET CURRENT REDUCTION STRATEGIES

Three main axes have been highlighted so far in the literature for reducing the reset current of analytical PCM cells: device scaling, cell structure engineering and PC material optimization.

Regarding the **device scaling**, I_{rst} is actually expected to scale down when shrinking the size of the active volume to be heated up to the melt. For example, in the particular case of lance-type structures which we are studying, the melted region corresponds to a cap located at the heater's tip and the reset current has been shown to decrease when scaling down the dimensions, following at first order a linear variation with the surface of the electrical contact. [6] Meanwhile, thermal losses induce deviations from this linear behavior when shrinking down to very low values the heater's dimensions. [7]

The **cell structure** is obviously an other key factor likely to have a large impact on I_{rst} , since it governs the heat dissipation in the PC layer. Together with Joule heating, heat dissipation is a main parameter controlling the temperature increase in the PC layer during the reset operation. For example, it has been shown that the so-called confined structure minimizes the thermal losses as compared to the lance-type structure resulting consequently in lower I_{rst} . [8]

Finally, **PC materials engineering** has also been proposed for reducing I_{rst} . For example, additions of SiO_2 into a $\text{Ge}_2\text{Sb}_2\text{Te}_5$ matrix have been shown to result in large I_{rst} reductions, [9] which are believed to result from the modification of both the electrical and the thermal characteristics of the PC material. The different physical parameters that determine the current required to reset the cell can be identified throughout a review of the physical effects that play a role in the reset mechanism.

First, let's consider the heat source warming up the PC material during the reset pulse, ie the **Joule heating**. Generally speaking, the Joule heating during the reset pulse can occur both in the heater and in the PC layer. In our devices that are lance-type structures with a cylindrical W heater of diameter and height equal to 300nm while the PCM layer is a 100nm thick chalcogenide film (Figure 1), the heater gives a very small contribution to the PC layer temperature increase due to both its low electrical resistance and low thermal efficiency. In such self-heating PCM cells, the temperature reached inside the PC layer mainly depends on the power developed inside the PC layer, which is directly linked to the electrical characteristics of the PCM material. Typical PC materials show a non-ohmic behavior characterized by an increase of the electrical conductivity with increasing electric field. The power developed in the PC layer is hereafter the sum of two contributions, the ohmic part which is determined by the on-resistance of the chalcogenide layer R_{on} and the non-ohmic part which is determined by the holding voltage V_h . [10]

Next, to further identify which physical characteristics of the PC material will determine I_{rst} , we have to consider the **heat dissipation** during the reset pulse, which can be evaluated from the heat transfer equation. The heat dissipation comprises the change in energy following the temperature increase of the PC layer up to the melting temperature T_m and also the thermal loss due to heat diffusion. Modifications of the PC material will affect the heat dissipation required to achieve melting of the PC material, through various parameters like the melting temperature T_m , the specific heat C_p , the latent heat of fusion L_f or the thermal conductivity k_{th} . [11]

Finally, it is also important to consider the behavior of the PC material during the **quench period** which occurs just after the reset current has been switched off. In the case of a PC material with a large crystalline growth speed v_G , it has been demonstrated that a certain portion of the PC material located at the periphery of the melted volume can recrystallize during the quench. The amorphous volume ends up being then much smaller than the melted volume, and overheating largely above the melting is required to end up in the high resistance state. For example, the reduction of

I_{rst} following the decrease of the Sb to Te ratio in Ge-doped SbTe PCM cells is the result of the decrease of the growth speed. [12]

In summary, reset current reductions can be achieved with device scaling and cell structure optimization, by allowing a better electrical and thermal confinement within the structure. Meanwhile, modifications of the electrical, thermal, and thermodynamical characteristics of the PC materials will also affect the reset current by altering the heat source or the heat dissipation.

3. Reset current reduction using a thin interfacial oxide layer [1]

As a first example illustrating the reduction of the reset current of PCM cells, we present here the results obtained with the introduction of a thin interfacial oxide layer. HfO_2 layers of thickness 2nm or 3nm have been introduced in lance-type structures illustrated in Figure 1, between the top of the W plug (300nm in diameter and height) and the $Ge_2Sb_2Te_5$ layer (100nm in thickness). As expected, the cells with the oxide layers are found to be initially in a much higher resistance state than the reference cells having no oxide layers, due to the insulating characteristics of the oxide layer. As a forming procedure, a staircase up sequence of pulses is first applied to the cells to switch the devices to a low resistance state. During this procedure, a sharp decrease of the cell resistance is occurring at a breakdown voltage of about 4V and 5V respectively for the devices with a 2nm and 3nm thick oxide layer, and it is attributed to the formation of some localized conductive filaments in the oxide layer. Figure 2 shows the programming characteristics of the devices, as evaluated after the forming step. The introduction of the oxide layer is found to result in large current reductions: the devices with the 2nm and 3nm HfO_2 layers exhibit a reduction of the reset current respectively of the order of 60% and 40% as compared to the reference cells having no oxide layers. Our results also show the good endurance performances of the devices with the interface layer, with the demonstration of up to more than 10^7 cycles.

As for the origin of the reduction of the reset power and current, we can first envisage the better thermal efficiency of the devices having an oxide layer, which is likely to limit the thermal dissipation toward the conductive W plug during the reset operation. However, the best thermal efficiency would be expected with the thicker 3nm oxide layer, resulting in this case to the largest power reduction, which is not observed experimentally. So the improved thermal efficiency of the devices with the oxide layer cannot be the unique explanation giving account for the power and current reduction observed during the reset operation. The other parameter having been modified with the introduction of the interfacial oxide layer is the dimension of the effective contact surface, which is directly related to forming procedure. In fact, the smaller forming voltage of the thinnest 2nm oxide layer has likely induced smaller filaments because of the smaller current peak flowing through the oxide during the forming procedure. Assuming the same current density for the devices with and without the oxide layer (ie the same thermal efficiency for the two structures) we can estimate the diameter of the effective contact surface to be equal to 190nm and 230nm respectively for the 2 and 3nm thick oxide layers, instead of 300nm for the reference cell having no oxide layer. A better control of the current peak during the forming procedure could further reduce the size of the effective contact surface and hereafter the value of the reset current.

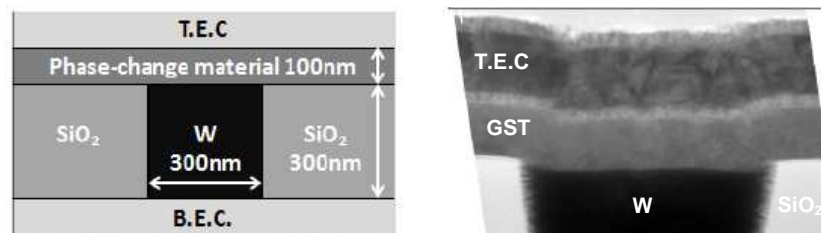


Figure 1: Schematic drawing and TEM cross-section of the lance-type structures under study.

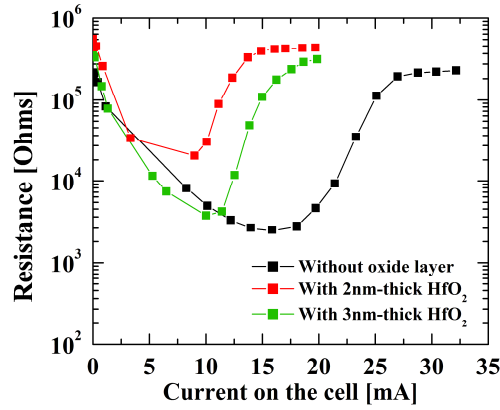


Figure 2: $R(I)$ program curves for the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ devices without and with a thin interfacial HfO_2 layer of thickness 2 and 3nm.

4. Lowering the reset current with carbon-doped $\text{Ge}_2\text{Sb}_2\text{Te}_5$ [2]

We have next investigated the effect of carbon additions into $\text{Ge}_2\text{Sb}_2\text{Te}_5$, and we present here a focus on the results obtained with 5% carbon. The films have been deposited by co-sputtering from two pure targets of GST and Carbon and lance-type cells have been fabricated and characterized. As can be seen on the programming curves displayed on Figure 3, the addition of 5% Carbon in the GST material results in a pronounced reduction of the reset current of more than 50%, while the reset power $V_h \cdot I_{rst} + R_{on} \cdot I_{rst}^2$ dissipated in the PC layer is reduced by about 25%. In this case, the reset current reduction cannot be accounted for by a modification of the contact surface dimension following the addition of carbon. Here, to explain the reset power reduction, we have to envisage either a better thermal efficiency of the cell achieved through a reduction of the thermal conductivity of the PC material or a reduction of the energy required to reach the melting temperature through a variation of various physical parameters (T_m , C_p , L_f). In other phase change materials, the respective contribution of these two effects has been successfully evaluated thanks to measurements of the melting current as a function of the temperature. [13]

On top of the reduction of the reset power, which follows the reduction of the non-ohmic contribution $V_h \cdot I$ of the self-heating power of the materials, our characterization of carbon-doped devices reveals an increase of the value of the holding voltage V_h from 0.49V to 0.72V. In this system, both the decrease of the necessary power to reset and the increase of the holding voltage are shown to account for the reset current reduction obtained with the addition of carbon into $\text{Ge}_2\text{Sb}_2\text{Te}_5$.

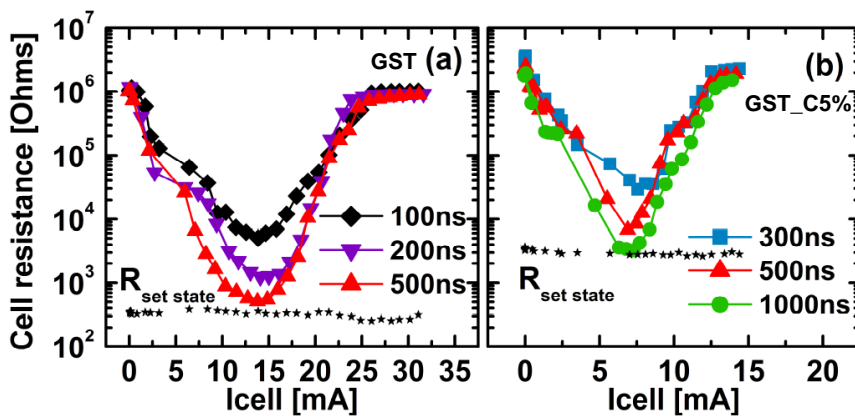


Figure 3: $R(I)$ program curves for (a) the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ reference devices and (b) the $\text{Ge}_2\text{Sb}_2\text{Te}_5 + 5\text{at}\% \text{C}$ devices.

5. Electrical performances of $\text{Ge}_x\text{Te}_{1-x}$ Phase Change Memories [3]

As a last example and to further illustrate the strategies available to reduce the reset current of PCM devices, we review here the electrical performances of PCM cells made of Ge_xTe_y films with various stoichiometries. The PC layers have been obtained from the co-sputtering of two pure Ge and Te targets, resulting in a Te content ranging from 50 to 70at%. The programming curves of the lance-type PCM cells displayed in Figure 4 show that the reset current necessary to reach the maximum resistance is reduced by about 30% when going from 50 to 70at% Te. In this series of data, TEM pictures reveal that the crystallization velocity plays a primordial role in the determination of the reset current I_{rst} , as it has already been reported in other cases of fast growth PC materials. [12]

Let's first focus on the programming curves of the $\text{Ge}_{50}\text{Te}_{50}$ compound. Pulses as short as 50ns can be used to achieve the low resistance state with more than 2 orders of magnitude for the resistance contrast, thus confirming a high crystalline growth speed of the material. [14] TEM imaging performed for different programming currents reveal that this very fast crystallization velocity induces a recrystallization phenomenon at the surface of the plug during the reset operation. As a result, for long pulse duration of more than 300ns, the programming curves show a non-monotonic behavior with increasing programming currents, and the reset current necessary to achieve the maximum resistance ($\sim 46\text{mA}$) is well above the melting current ($\sim 24\text{mA}$).

When increasing the Te content to 70at%, we observe a much smaller crystallization speed, which is illustrated by the much longer pulse durations required to achieve the full crystallization and which is also reported in the literature. [15] No recrystallization phenomenon is likely to occur with such a low crystallization speed, as also indicated by the monotonic behavior of the programming curves, thus resulting in a lower reset current that matches in this case the melting current.

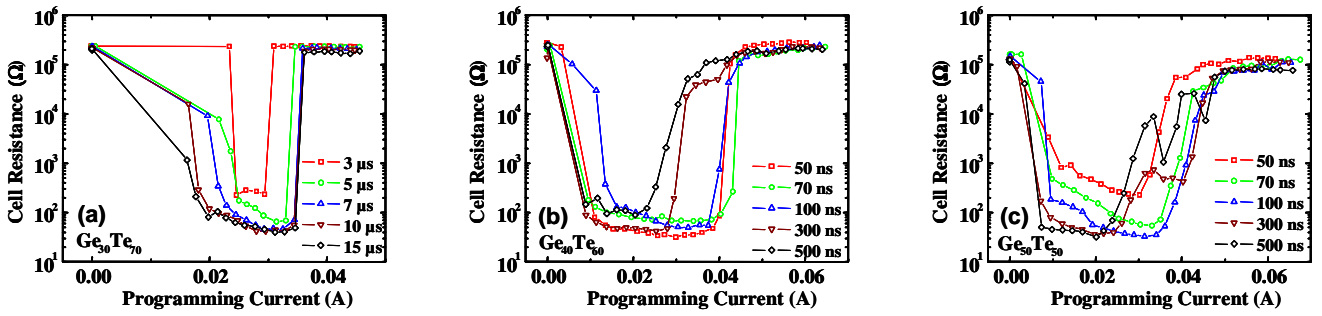


Figure 4: $R(I)$ program curves for the $\text{Ge}_x\text{Te}_{1-x}$ devices with various stoichiometries:

(a) $\text{Ge}_{30}\text{Te}_{70}$ (b) $\text{Ge}_{40}\text{Te}_{60}$ (c) $\text{Ge}_{50}\text{Te}_{50}$

6. CONCLUSIONS

We have illustrated several strategies allowing reducing the reset current of analytical PCM cells. Large I_{rst} reductions have been experimentally demonstrated and interpreted in terms of a decrease of the electrical contact aperture, an increase of the holding voltage or a decrease of the crystallization speed. Other parameters are also likely to play a role in the observed reset current reduction (e.g. T_m , C_p , L_f , k_{th}), however experimental data on those are not easy to obtain since we need here to consider the variation of those parameters with the temperature. The determination of the relative contribution of all these parameters to the reduction of the reset current is likely to rely both on their experimental evaluation (including their temperature dependence) when achievable, and on the use of multiphysical simulations.

To conclude, we would like to mention that although the reset current is a crucial parameter to be considered among the programming characteristics of PCM devices, one should also take into account other important characteristics like for example the energy necessary to set the cell. Moreover, on top of an analysis of the RESET and SET characteristics at the cell level, rigorous investigations should be enlarged to a global analysis at the system level, where solutions for optimizing power consumption can also be found.

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Biography

Véronique Sousa graduated in 1994 from the Institut National Polytechnique de Grenoble (INPG) in the field of Materials Science and Engineering. During her PhD, which she received in 1997 from the INPG, she worked on the experimental and fundamental aspects of magnetic thin films with perpendicular anisotropy and spent a 3 months stay at the Electrotechnical Laboratory, in the group of Prof. Katayama, to work on magneto-optics. Afterwards, she took a one-year post-doctoral position at INESC in the group of Prof. P. Freitas, and worked on various thin film materials used for magnetic data storage devices such as permanent magnets, spin valves or tunneling junctions. Since October 1998, she is working at CEA-Leti-MINATEC-Campus where she first focused on the development of advanced magneto-optical and phase change materials for optical data storage. Hereafter, she managed several projects aiming at the optimization of chalcogenide materials for various solid state memory technologies, including Current Bridging RAM and Phase Change Memories.