Crystallization phenomena in phase change memories: non-Arrhenius kinetics, modeling and novel applications

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ABSTRACT

Phase change memory (PCM) operation relies on phase transition induced by electrical pulses, namely melting and crystallization. To predict and optimize the programming dynamics of PCM, detailed numerical models of pulsed-induced crystallization are therefore needed. In this work, we study the crystallization kinetics in $Ge_2Sb_2Te_5$, comparing the thermal regime (low temperature) and the set regime (high temperature) in PCM devices at 90 nm technology. The crystallization kinetics is shown to be dictated by two different energetic barriers, with a low activation energy E_x = 0.5 eV at high temperature. The non-Arrhenius temperature dependence of the crystallization rate is attributed to the fragile nature of the chalcogenide amorphous phase. We show a new crystallization model that includes nucleation, growth and the different energy barriers at low and high temperature, capable to predict the phase transition in both the thermal and set regimes. Finally, novel Boolean logic applications enabled by fast and controllable crystallization in PCM are discussed. It is shown that crystallization, together with threshold switching and amorphization, allows for a functionally complete logic operation in PCM.

Key words: PCM, crystallization, phase transition, chalcogenide materials, Arrhenius kinetics, Boolean, logic, normally-off logic.

1. INTRODUCTION

Phase change memory (PCM) is among the most promising emerging memory technologies, since it shows high switching speed [1, 2], low programming voltages and sub-decananometer scaling [3, 4]. The logic information in PCM is stored as the resistance *R* of a chalcogenide material, usually $Ge_2Sb_2Te_5$ (GST), which is capable of switching from a high resistivity amorphous phase (reset state, few MΩ) to a low resistivity poly-crystalline phase (set state, kΩ). The PCM operation relies on the phase transition induced by electrical pulses, namely melting and crystallization. Both are thermally-driven processes, in that they are controlled by the local temperature. For instance, melting takes place when the local temperature exceeds the melting point for the chalcogenide material, allowing the subsequent freezing into the amorphous phase. Melting and amorphization are fast processes (< 50 ns), which are limited by the electrical and thermal delays needed to raise the local temperature to/above the melting point. On the other hand, crystallization is comparably slower (>100 ns [5]), since the atomic ordering proceeds through statistical nucleation and growth phenomena with well-defined energetic barriers. Faster crystallization has also been reported in the few ns [1] and sub-ns regime [2], although for specific materials and/or electrical operation, *e.g.*, priming. To predict and reduce the crystallization time, a better understanding of the crystallization kinetics is required. Several works have addressed crystallization in the thermal regime, namely T < 200°C and t > 1 s in GST [6–9]. Most recently, ultrafast crystallization experiments have highlighted non-Arrhenius crystallization in GST [10]. This work discusses the crystallization mechanism in PCM devices, providing evidence for non-Arrhenius kinetics in GST. A numerical model is presented, capable of predicting the crystallization time in both the thermal and set regimes, with two different activation energies. Finally, we describe novel Boolean functions in PCM, where crystallization acts as the enabling process for computation [11].

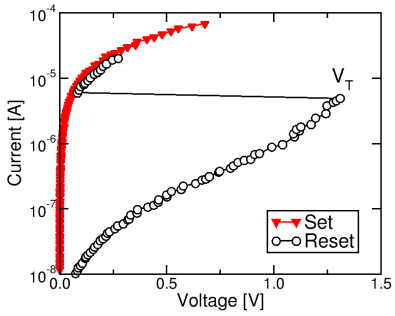

Fig. 1 Measured I-V characteristics of a PCM device in the set and reset states. The set state (solid triangle) shows a low-resistance ohmic behavior. The reset state is characterized by a highly non-linear subthreshold (OFF) region, culminating at the threshold voltage V_T where a sudden transition to the ON state (threshold switching) takes place.

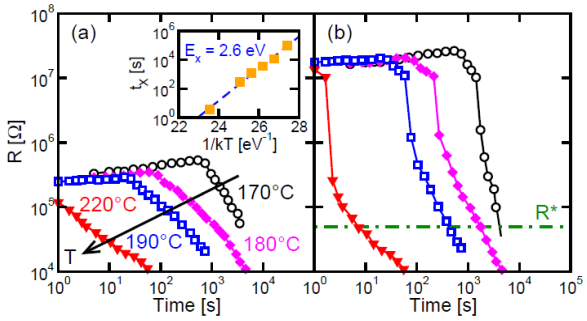

Fig. 2 Measured (a) and normalized (b) R as a function of annealing time for a reset state at increasing annealing temperature T. The resistance R in (a) was normalized to room temperature (300 K) in (b) according to (1). The crystallization time t_x was defined as the crossing of each normalized R curve at R_ = 50 kΩ. The Arrhenius plot of crystallization times in the inset of (a) shows a clear Arrhenius behavior, with an activation energy E_x = 2.6 eV.

2. EXPERIMENTAL RESULTS: THERMAL REGIME

Fig. 1 shows the measured I-V curves of a PCM device for the set and reset state, indicating the different resistance R and the characteristics threshold switching at a voltage V_T in the reset state [12]. The transition to the reset state is achieved through melting induced by Joule heating and fast quenching from the liquid phase. On the other hand, transition to the set state is achieved by application of a voltage pulse which induces Joule heating and a consequent nucleation and growth of the crystalline phase.

Crystallization was evaluated on 90 nm PCM devices with GST active material [12]. To study the kinetics of crystallization in the thermal (annealing) regime, PCM devices in the reset state were subjected to isothermal annealing conditions at constant temperature T and increasing times. Fig. 2a shows the measured R as a function of annealing time for a PCM initially programmed in the reset state. The resistance first gradually increases due to drift induced by the structural relaxation [13], then decreases as the crystallization takes place. In the experiment, the resistance was measured at the annealing temperature. To extract the crystallization time t_x, we normalized the measured resistance at room temperature in Fig. 2b according to an Arrhenius law for the T-dependence of R with activation energy of 0.25 eV [14]. The crystallization time t_x, evaluated in correspondence of the crossing at R* = 50 kΩ, decreases for increasing annealing temperature T from 170 to 220°C. The inset shows the measured crystallization time t_x as a function of 1/kT: Data indicates an Arrhenius behavior according to:

$$t_x = \tau_0 e^{\frac{Ex}{kT}} \qquad (1)$$

where $\tau_0 = 3\times10^{-26}$ s is the pre-exponential factor, k is the Boltzmann constant and E_x = 2.6 eV is the activation energy for crystallization. These results are in agreement with previous experimental data, all showing a relatively high activation energy above 2 eV for crystallization in GST. Note that it is this high E_x that allows strong data retention in PCM, usually in the range of 10 years for operation temperature of about 100°C [15].

3. SET KINETICS

The crystallization kinetics was also studied in the set regime, where crystallization is induced by the electrical pulses responsible for Joule heating in the PCM device. Set experiments were performed in integrated one-transistor/one-resistor (1T1R) structures, where the PCM is connected in series with a

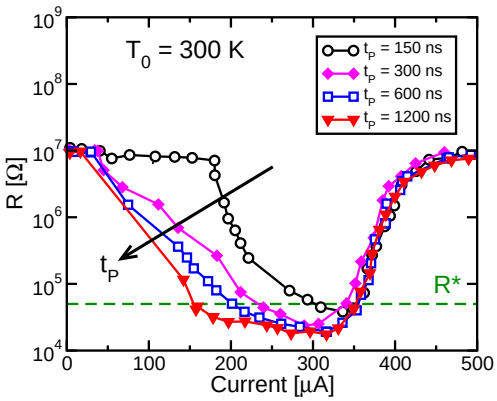

Fig. 3 Programming characteristics showing R as a function of the current of the applied pulse, for T_0 = 300 K. Curves are shown for increasing pulse width t_P. The crystallization current is extracted in correspondence of the crossing at the threshold resistance R^* = 50 kΩ.

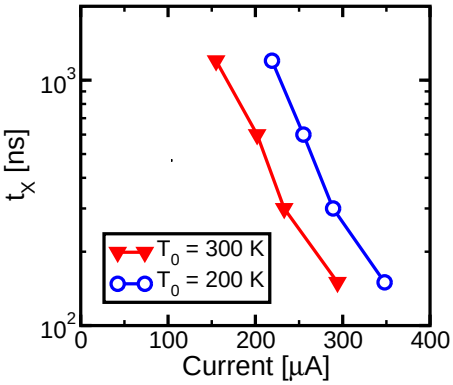

Fig. 4 Measured t_x as a function of the programming current I for ambient temperatures T_0 = 200 and 300 K. The crystallization time t_x and the corresponding current I were taken as the pulse time t_P and the current for which $R = R^*$.

MOSFET selector. By biasing the MOS transistor at a fixed gate voltage V_G, we were able to control the current during programming, corresponding to the saturated drain current of the MOSFET device. This allowed avoiding current overshoots at threshold switching due to the parasitic capacitance C_P [16]. Fig. 3 shows the R-I programming curves, namely the resistance R measured after application of a pulse with current I and pulse-width t_P at room temperature (T_0 = 300 K). Rectangular pulses with width between 150 ns and 1.2 μs were applied to electrically induce crystallization. The pulse current was evaluated from the saturated current of the MOSFET at the corresponding gate bias. The R-I curve shows a decrease of R for increasing current I below the melting current I_m = 320 μA, followed by a R increase above I_m. The R decrease is due to crystallization in the solid state, while the increase above melting marks the onset of amorphization from the liquid phase.

We concentrated on the regime $I < I_m$ to study electrically-induced crystallization. For any given I in the crystallization (set) regime, R decreases for increasing t_P due to time-dependent growth of crystalline domains within the amorphous phase. Therefore, as the current is increased, a larger amount of crystallized phase is established for any given time. Conversely, the crystallization time decreases for increasing current, as reported in Fig. 4, showing the crystallization time as a function of the pulse current from Fig. 3. The crystallization point was defined at a critical R* = 50 kΩ, as in the inset of Fig. 2. The crystallization time was evaluated at two ambient temperatures T_0, namely T_0 = 200 and 300 K: the t_x-I curve shifts to higher I for decreasing T_0, since more Joule heating is needed to heat up the PCM volume to a characteristic crystallization temperature, as T_0 is decreased.

4. JOULE-HEATING MODEL

Results in Fig. 4 (set regime) should be reported as a function of the local temperature, to check whether crystallization in the set regime obeys the same kinetics as in the thermal annealing (Fig. 2). To convert the programming current into the local temperature, we developed a Joule heating model to describe electrically-induced heating during the set pulse in the reset-state PCM structure of Fig. 5. The simulated mushroom structure has a cylindrical symmetry that allows 2D-reduced simulations. Current continuity and Fourier equations were solved to evaluate the current density and temperature distributions. the temperature-dependence of electrical and thermal conductivity in the crystalline phase were considered, to allow self-consistent calculations of current, field and temperature [12]. Poole-Frenkel transport was assumed in the amorphous phase, which nicely accounts for I-V curves in sub-threshold region at increasing T_0 from 150 to 300 K in Fig. 6. Threshold switching was modeled as the electronic transition to high conductivity in the conductive channel through the amorphous

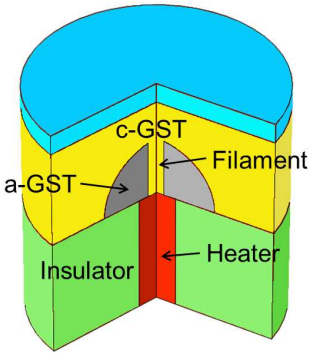

Fig. 5 Schematic illustration of the simulated PCM structure. The filament describes the high-conductivity (ON) state of the amorphous phase after threshold switching.

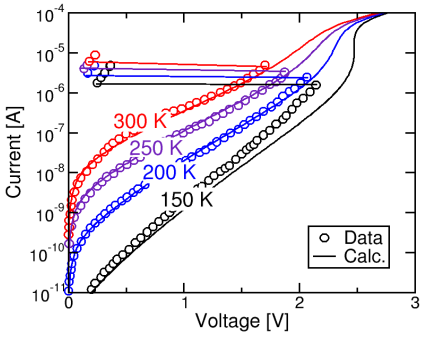

Fig. 6 Measured and calculated I-V curves for the full-reset state at increasing T_0 from 150 to 300 K.

volume in Fig. 5. In the conductive channel, the electrical conductivity σ and the thermal conductivity k_{th} were the same as in the crystalline GST [17]. Filamentary switching is consistent with the general explanation of breakdown phenomena, where the conductivity enhancement takes place at the point of maximum field and/or maximum current density. For the sake of simplicity, the filament was assumed to be located in correspondence of the central axis of the simulated structure in Fig. 5. The filament diameter was assumed to increase for increasing current thus allowing to account for the experimental I-V characteristics after threshold switching in Fig. 7.

Fig. 8 shows the calculated effective temperature, namely the temperature at the interface between the bottom electrode and the chalcogenide volume, as a function of the programming current. The effective temperature was calculated for both the set state (crystalline phase) and for the reset state, consisting of the mixed phase configuration in Fig. 5. Localized conduction in the filament leads to strong Joule heating, which is responsible for the local crystallization. The effective temperature is higher in the reset state, due to the low thermal conductivity in the amorphous phase and the localized conduction in the channel, both providing conditions of higher electrical/thermal confinement in the device. The effective temperature was the smaller temperature within the conductive channel, thus describing the limiting step for completion of the crystalline channel during the set transition. Note that there is a temperature difference of about 100°C between the effective temperature evaluated at T_0 = 200K and 300 K, which confirms the good accuracy of our results. Also note that the calculated temperature is equal to T_m in correspondence of the experimental values for the melting current I_m = 320 μA for T_0 = 300 K and I_m = 370 μA for T_0 = 200 K, again supporting the consistency of the results of the Joule heating model with the experimental characteristics.

5. NON-ARRHENIUS CRYSTALLIZATION

From Fig. 8, the effective temperature T can be extracted at any applied I, allowing the comparison of the crystallization times in the thermal regime (Fig. 2) and the set regime (Figs. 3 and 4). Fig. 9 shows the Arrhenius plot of t_x for GST-based PCM, collecting the thermal annealing data in the inset of Fig. 2 and data in Fig. 4 after conversion of I into the effective temperature. Thermal annealing data from other works are also reported for reference [10, 18]. Data do not show a single slope in the Arrhenius plot, rather two values for the activation energy E_x are obtained for the thermal regime (E_x = 2.6 eV) and the set regime (E_x = 0.35 eV). These results provide evidence for non-Arrhenius crystallization in PCM, in agreement with previous ultrafast calorimetric results [10]. Note that set-regime t_x for T_0 = 200 K and 300 K overlaps in Fig. 9, thus suggesting that set-regime crystallization is a thermally-driven process, with negligible impact of electrical effects such as current-driven electromigration [19] or field-induced nucleation [20]. Data are compared to previously reported t_x for thermal crystallization in line-type PCM (E_x = 1.85 eV) [18] and to measured viscosity in powdered $Te_{85}Ge_{15}$ (E_x = 0.34 eV) [10]. These data are consistent with non-Arrhenius crystallization, where different

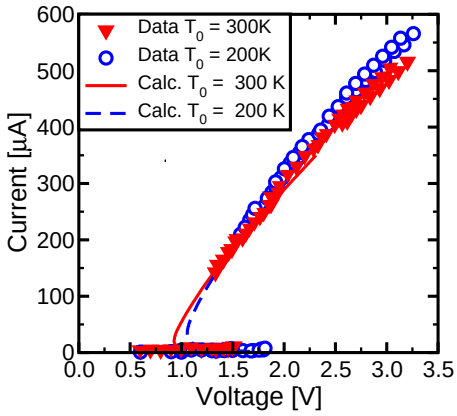

Fig. 7 Measured and calculated I-V characteristics at T_0 = 300 K and 200 K. Filamentary conduction above threshold switching can account for the ON-state behavior.

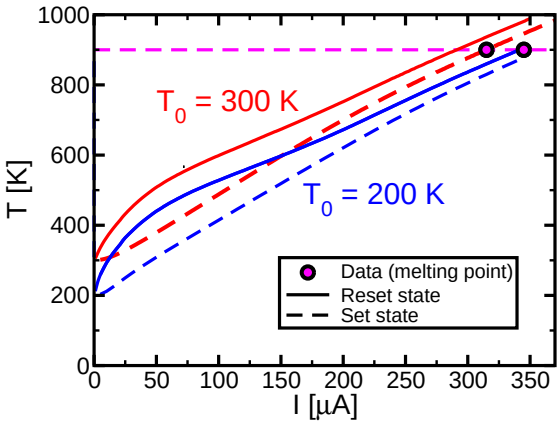

Fig. 8 Calculated effective T at the heater-GST interface as a function of I for T_0 = 200 K and 300 K. Simulation results are shown for the set state and for the reset state in the ON state. The model is able to capture the measured melting currents I_m at T_0 = 200 K and 300 K in Fig.3.

values of E_x are obtained above/below about 300°C. The non-Arrhenius behavior can be attributed to the fragile nature of the GST glass [10], which can be due to the breakdown of Stokes-Einstein relation as the triggering event of fast crystallization in fragile liquids [21]. The two distinct activation energies for crystallization at high/low temperature allows markedly different behaviors under data retention and set regime.

The strong T-dependence of crystallization rate in the thermal regime allows to achieve good data retention, i.e. long crystallization time at relatively high temperatures, and fast programming, namely short crystallization times at temperature above 300°C, which are reached during the programming pulse by Joule heating. At the same time, the crystallization rate in the set regime shows a relatively weak T dependence, which allows a good controllability of phase change. For instance, changing the programming current from 150 µA to 300 µA in Fig. 4 results in a change of t_x by less than a decade. This allows a fine control of the crystallization state, which might be helpful for specific applications such as multilevel PCM [22-24], spike timing dependent plasticity [25] and logic computing [11, 26, 27].

6. PCM LOGIC ENABLED BY CRYSTALLIZATION

To illustrate the capability to perform logic operations in Boolean algebra with PCM, we describe summation and NOR operation in a single PCM device [11]. In this computing approach, the PCM device is used as a state machine, where consecutive input pulses modify a state variable (the threshold voltage V_T). The final value of the state variable is a function of the input pulses, thus establishing a logic gate with extremely small area (single PCM cell) and nonvolatile behavior, thus allowing a normally-off operation with virtually zero static power consumption [30].

Fig. 10a shows the measured V_T, namely the state variable of the PCM, as a function of the duration of a crystallizing pulse. The latter is schematically shown in the inset of Fig. 10 and consists of two rectangular pulses: The first is a 70-ns pre-pulse to induce threshold switching and bring the PCM in the conductive ON state, the second is a crystallizing pulses with fixed amplitude (V_P = 1.5 V) and variable duration t_{cryst}. This second pulse that is responsible for moderate Joule heating at relatively low voltage to establish a controlled crystallization. V_T decreases for increasing t_{cryst} due to the time-dependent nucleation and growth in the PCM [28, 29]. This is shown by numerical simulations of crystallization in Fig. 11, showing the temperature profile (top) and the crystalline fraction (bottom) for increasing times, namely t_{cryst} = 0 ns (b), 50 ns (c), 100 ns (d) and 150 ns (e). The numerical model extended the Joule heating model of Sec. 4 with a T-dependent crystallization rate, described by:

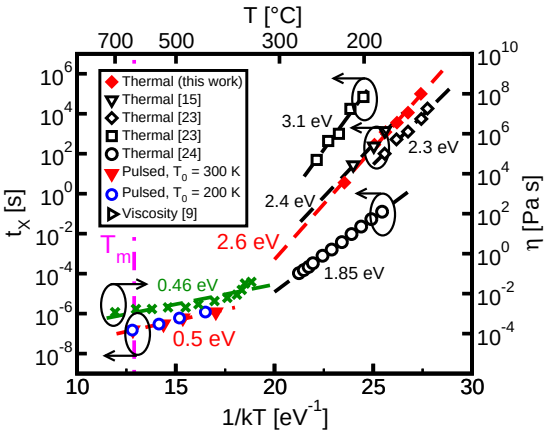

Fig. 9 Arrhenius plot of t_x for the thermal regime (same data as in Fig. 2) and the pulsed regime. Data indicate different E_x for the thermal regime (E_x = 2.6 eV) and for the pulsed regime (E_x = 0.5 eV), thus evidencing non-Arrhenius crystallization in PCM. PCM data are compared with thermal annealing data for mushroom cells [16], [24] and line-type PCM [25]. High-temperature viscosity data in powdered $Te_{85}Ge_{15}$ are also shown for reference [9].

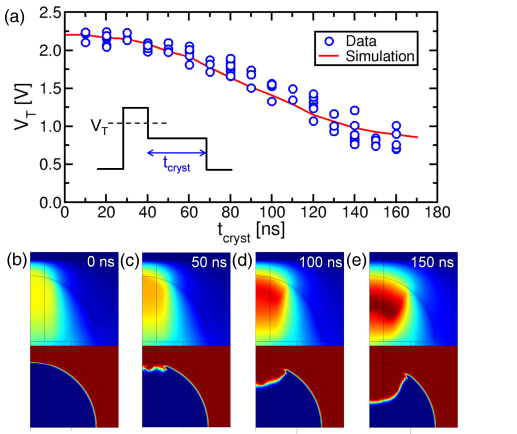

Fig. 10 (a) Measured V_T as a function of the crystallizing time t_{cryst} in the applied pulse shown in the inset. The pulse consists of a short high-voltage pre-pulse inducing threshold switching, followed by a constant lower voltage causing Joule heating and crystallization. The decrease of V_T for increasing t_{cryst} indicates additive crystallization in the PCM. (b-e) Calculated map of temperature (top) and of crystalline fraction (bottom) for increasing t_{cryst} = 0, 50 ns, 100 ns and 150 ns. The crystalline phase grows for increasing time, leading to the observed decrease of V_T (a) and R (not shown).

$$\frac{df}{dt} = \frac{1-f}{\theta} e^{-\frac{E_x}{kT}} \left(\left| \frac{\partial^2 f}{\partial^2 r} \right| + \left| \frac{\partial^2 f}{\partial^2 z} \right| \right), \qquad (2)$$

where $\theta = 5.2 \times 10^6$ sm^{-2} is a characteristic constant. The term in the parenthesis is a correction function to enhance growth at the boundary between crystalline and amorphous phases, where the curvature of *f* is relatively large. As the crystallization proceeds, the thickness of the amorphous volume decreases, thus V_T decreases in Fig. 10a.

The gradual decrease of V_T by applied pulses can be used to perform addition in a single PCM device, as experimentally demonstrated in Fig. 11 for a PCM device with doped $Ge_2Sb_2Te_5$. Addition is achieved in a sequence of three steps: In the first step, the PCM is initialized in the high resistance state, conventionally identified at state M = 1 (high V_T). initialization is achieved through a reset pulse, where the PCM is heated above the melting point and suddenly quenched into the amorphous phase. After amorphization, the second step is consists of the compute phase, where the two input pulses X_1 and X_2 are applied. The two pulses X_1 and X_2 carry the input logic signals, namely a high amplitude above V_T consists of a high binary input value (M = 1), while a low amplitude below 0.5 V corresponds to a low input value (M = 0). A crystallizing pulse-width t_{cryst} = 120 ns was used in the experiments. Figs. 11a-d show the sequence of initialize and compute phases for the four combinations of X_1 and X_2, which are considered in the following:

- For $X_1 = X_2 = 0$ (Fig. 11a), the PCM remains in its original state (M' = M = 1), since the applied pulses never exceed threshold voltage. The threshold voltage also remains at its original high value of about 2.2 ns. The final state is visualized by the measured I-V curve in red (M' = 1) in Fig. 11e.

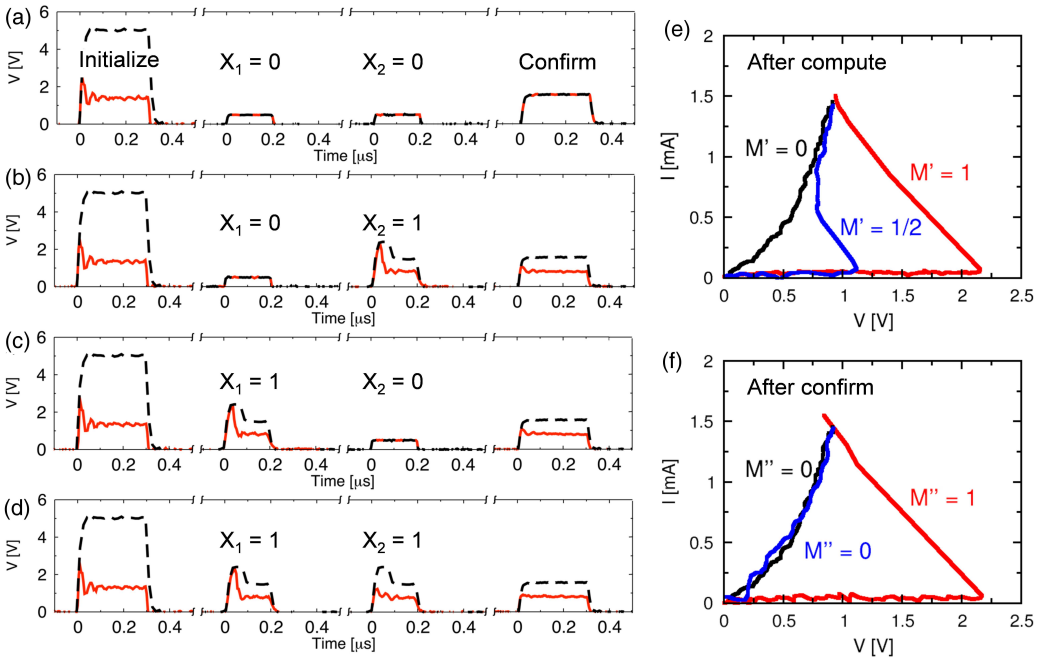

Fig. 11 (a-d) Measured applied voltage V_P and voltage across the cell during initialize and compute for the four cases of logic inputs X_1 and X_2. The initialize pulse prepares the PCM in state M = 1, which is then partially/totally crystallized in the compute phase depending on logic inputs. (e) Measured I-V curves after the compute phase for PCM states M' = 1 ($X_1 = X_2 = 0$), M' = ½ ($X_1 = 0$, $X_2 = 1$ or vice versa) and M' = 0 ($X_1 = X_2 = 1$). (f) Measured I-V curves after confirm, where the intermediate state M' = ½ is fully crystallized into state 0.

- For $X_1 = 0$ and $X_2 = 1$ (Fig. 11b), the PCM is partially crystallized, causing only a partial decrease of V_T to about 1.1 V, corresponding to state M' = ½. This state is visualized by the blue I-V curve in Fig. 11e.

- For $X_1 = 1$ and $X_2 = 0$ (Fig. 11c), the PCM is partially crystallized to state M' = ½, similar to the previous case. This state is visualized by the blue I-V curve in Fig. 11e.

- Finally, for $X_1 = X_2 = 1$ (Fig. 11d), additive crystallization leads to $V_T = 0$ and M' = 0. This is visualized by the black I-V curve in Fig. 11e.

Clearly, binary computing requires that only two logic state are achieved, thus the intermediate state M' = ½ must be reduced to 0 by the confirm phase. This consists of a pulse with amplitude $V_P = 1.5$ V which selectively induces full crystallization only for $V_T < V_P$, namely for state M' = ½. State M' = 0 is already in a fully crystalline phase, thus the applied pulse does not affect this state. Fig. 11f shows the I-V curves obtained after confirm for different input values. The intermediate state M' = ½ states is confirmed to M'' = 0. The final state variable M'' is thus always low, except for both inputs being low. This corresponds to the Boolean function M'' = NOR(X_1, X_2), Through a similar approach, also NAND and NOT operation can be experimentally demonstrated. This demonstrates functionally complete logic operation in a single PCM device, thus characterized by an extremely small area occupation and by a nonvolatile behavior, namely the computed output is retained in the PCM until further pulses are applied. This may allow for large reduction of the power dissipation, since the device is accessed only during dynamic computing, and does not require any bias for sustaining the computed state.

REFERENCES

[1] G. Bruns, *et al.*, *Appl. Phys. Lett.*, vol. 95, p. 043108, 2009.
[2] D. Loke, *et al.*, *Science*, vol. 336, pp. 1566–1569, 2012.
[3] S. H. Lee, *et al.*, *Nature Nanotech.*, vol. 2, pp. 626–630, 2007.
[4] F. Xiong, *et al.*, *Science*, vol. 332, pp. 568–570, 2011.
[5] D.Mantegazza, *et al.*, *Solid-State Electronics*, vol. 52, pp. 584–590, 2008.
[6] G. Ruitenberg, *et al.*, *J. Appl. Phys.*, vol. 92, pp. 3116–3123, 2002.
[7] S. Privitera, *et al.*, *J. Appl. Phys.*, vol. 94, p. 4409, 2003.
[8] J. A. Kalb, *et al.*, *J. Mater. Res.*, vol. 22, pp. 748–754, 2007.
[9] U. Russo, *et al.*, *IEEE Trans. Electron Devices*, vol. 54, pp. 2769–2777, 2007.
[10] J. Orava, *et al.*, *Nat. Mater.*, vol. 11, pp. 279–283, 2012.
[11] M. Cassinerio, *et al.*, accepted for publication in *Adv. Mat.*, 2013.
[12] N. Ciocchini, *et al.*, *IEDM Tech. Dig.* pp. 729–732, 2012.
[13] D. Ielmini, *et al.*, in *IEDM Tech. Dig.*, pp. 939–942, 2007.
[14] D. Fugazza, *et al.*, in *IEDM Tech. Dig.*, pp. 652–655, 2010.
[15] A. Redaelli, *et al.*, *IEEE Trans. Electron Devices*, vol. 53, pp. 3040–3046, 2006.
[16] D. Ielmini, *et al.*, *IEEE Electron Device Letters*, vol. 26, pp. 799–801, 2005.
[17] M. D. Pickett, *et al.*, *Nanotechnology*, vol. 23, p. 215202, 2012.
[18] S. Kim, B. Lee, *et al.*, in *Proc. IRPS*, 99–103.
[19] S.-W. Nam, *et al.*, *Science*, vol. 336, pp. 1561–1566, 2012.
[20] V. G. Karpov, *et al*., Appl. *Phys. Lett.*, vol. 90, p. 123504, 2007.
[21] G. C. Sosso, *et al.*, *Phys. Status Solidi B*, vol. 249, 2012.
[22] T. Nirschl, *et al.*, in *IEDM Tech. Dig.*, pp. 461–464, 2007.
[23] F. Bedeschi, *et al.*, in *ISCC Tech. Dig.*, pp. 428-625, 2008.
[24] G. F. Close, *et al.*, in *IEDM Tech. Dig.*, pp. 29.5.1 - 29.5.4, 2010.
[25] D. Kuzum, *et al.*, *Nano Lett.*, vol. 12, pp. 2179–2186, 2012.
[26] C. D. Wright, *et al.*, *Adv. Mater*., vol. 23, 2011.
[27] C. D. Wright, *et al.*, *Phys. Status Solidi B*, vol. 249, pp. 1978–1984, 2012.
[28] U. Russo, *et al.*, *IEEE Trans. Electron Devices*, vol. 54, pp. 2769–2777, 2007.
[29] Y. Shih, *et al.*, in *IEDM Tech. Dig.*, pp. 207–210, 2008.
[30] D. B. Strukov, *et al.*, in *ISCAS Proceedings*, pp. 1967 – 1970, 2010.

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