The Bridge Structure for Advanced Phase Change Memory Investigations

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ABSTRACT

This paper examines various aspects of phase-change memory studied on bridge cell structures. Although phase-change memory promises high speed, CMOS compatibility, System-on-a-Chip (SoC) compatibility, high endurance, and non-volatility, its high operating current remains a formidable challenge for solid-state memory applications. To reduce this current, several approaches have been proposed. Most of these improved structures rely on the reduction of the contact area between the bottom electrode contact and the phase-change material, and thus require difficult sub-lithographic processes to reduce the contact size between the electrode and the phase-change material. A phase-change bridge structure relieves the reliance on sub-lithographic processes and provides a fast path to rapid scaling. In this structure, a horizontal bridge of phase-change material connects two flat electrodes, so that the cross-sectional area is defined by the film thickness and the width of the bridge. Although the width of the bridge structure must be defined by lithography, a nearly identical process has long been used for CMOS gate patterning with good control of the critical dimension. Consequently, we have fabricated bridge devices with ultra-small cross-sectional area of 60nm^2 with RESET currents < 100 μA, demonstrating the scalability of phase-change memory.

In addition to the advantages of small operating current, the bridge device also provides a platform for investigating different materials and their scalability. Based on this structure, several research groups have studied the switching characteristics of doped and undoped $Ge_{15}Sb_{85}$ and doped SbTe, as well as $Ge_2Sb_2Te_5$-based material. We will examine the characteristics of the bridge cell when different phase-change materials are used.

Finally, since the bridge cell is a very delicate structure with minimum dimensions of only 3nm x 20nm, accurate testing by itself is a challenge. We will report a robust testing algorithm as well as testing results for various cells.

Key words:

Bridge Structure, GeSb, doped GeSb, SbTe, $Ge_2Sb_2Te_5$, feedback-control algorithm, PCRAM Scaling; PCRAM testing, PCRAM, PCM

1. INTRODUCTION

Phase-change solid-state memories have demonstrated the possibility for high speed, SoC compatibility, non-volatility, scalability and high endurance for vertical structures [1-3]. Although vertical-type devices occupy a smaller unit size and have been investigated extensively, lateral-type structures have also been introduced to investigate some key features of Phase-change Memory (PCM) such as new materials, crystallization behavior, and scaling [4-7]. A lateral line structure was first introduced to investigate the properties of doped SbTe, conveying the potential for such a lateral phase-change memory [4]. A lateral bridge structure was used to investigate the crystallization behavior of the $Ge_2Sb_2Te_5$ (GST) material with different initial conditions [7]. It was found that as-deposited material exhibited a longer crystallization incubation time and slower crystallization speed compared to melt-quenched phase-change material [7]. The bridge structure was also used to investigate the scaling properties of doped GeSb material, resulting in operational cells with very small cross-sectional area [6]. Figure 1 presents the two most investigated lateral structures for PCM devices, the line structure and the bridge structure. In the line structure, the phase-change material is deposited on a non-planar surface, due to the step-height of the underlying metal electrode. In contrast, the bridge

structure provides a flat surface for deposition of the phase-change material. Although the bridge structure involves a CMP (chemical mechanical polarization) process step, the flatness makes the structure a very good vehicle for studies of scaling and new materials. In addition, the electro-thermal effect was investigated with the bridge structure [5].

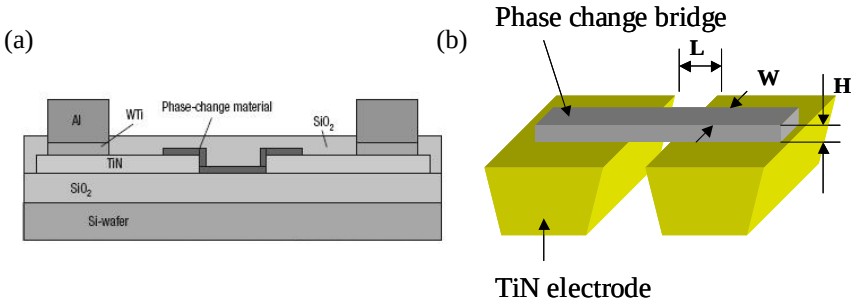

Fig. 1. Schematic drawings of two lateral-type phase-change memory device structures, including (a) the line structure [4] and (b) the bridge structure.

In this paper, we review the phase-change bridge structure, including the fabrication procedure, the potential areas of investigation, and the limitations of the structure. The achievements of our scaling studies are reviewed, and then studies where the phase-change bridge structure was used to investigate different materials, including doped SbTe, GeSb, and doped $Ge_2Sb_2Te_5$, are discussed. Finally, we discuss the testing system for the device. A flexible and accurate testing system is required to obtain reliable and accurate data. We introduce a new feedback-control algorithm to eliminate the pulse distortion, and obtain a flexible and highly controllable testing system enabling advanced investigations of the phase-change bridge as well as other phase-change memory devices.

2. EXPERIMENTS

Figure 2 illustrates the process flow to fabricate bridge devices. The two bottom electrodes were made by a TiN damascene process. The narrow slit of SiO_2 between the two electrodes was made possible by a trimming process. A Scanning Electron Microscope (SEM) picture after the TiN electrode fabrication process is shown in Fig. 2(b). The narrow oxide gap can be successfully defined using a KrF (248nm) based lithographic process. TiN was chosen for the electrodes because of its thermal stability, its compatibility with CMOS processes, and its inertness next to the phase-change material during repeated switching cycles. Ultra-thin (down to 3nm) phase-change material was then deposited on the wafer. An oxide with a thickness of 5-10 nm was then added to encapsulate the phase-change material and prevent oxidation. The bridge feature was then lithographically defined. For advanced devices, electron-beam lithography was used; exposing a silicon-oxide-based negative photoresist for patterning that is left as a hard-mask for subsequent processing. Ion milling was used to transfer the photoresist pattern into the phase-change layer. Cheng et al. evaluated the etching process for phase-change material ($Ge_2Sb_2Te_5$) and found that the Cl based etch generates, under many circumstances, undesirable porous film surfaces [8]. Although ion-milling is not a standard semiconductor manufacturing process, it can reduce the damaging effects of etching. Immediately after the ion-milling process, a 5-nm thick layer of silicon oxide was then deposited in situ on the wafer to protect the phase-change material from oxidation. The plane view SEM in Fig. 2(c) shows the bridge device after the etching and the encapsulation processes. The final step was deposition of a thick silicon oxide for protecting the device and wiring. The Transmission Electron Microscope (TEM) picture shown in Fig. 2(d) is an example of a bridge cell after a RESET operation.

The devices were tested with custom-made testers, ranging from systems that could provide only single square pulses to high-resolution testing systems with variable pulse profiles and complex testing sequences. Testing will be discussed in Section 3.3 below.

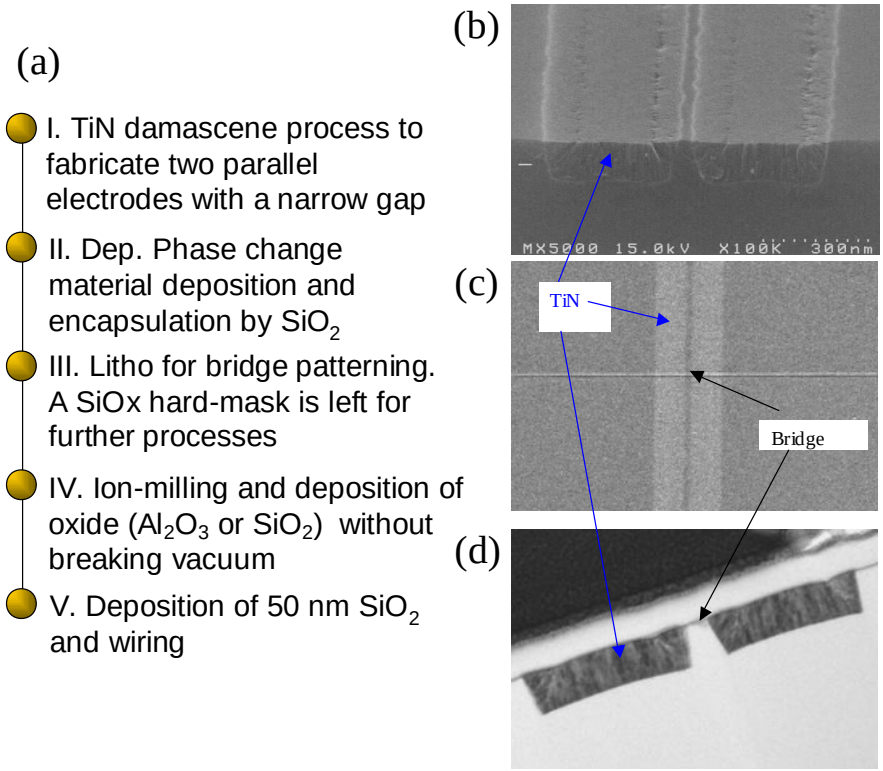

Fig. 2. (a) Process flow for fabricating a phase-change bridge device, (b) cross-sectional SEM of TiN electrodes after CMP (40nm gap between the two electrodes), (c) plane view SEM after step IV (20nm bridge width), (d) TEM picture of a device after testing (5-nm thick doped $Ge_2Sb_2Te_5$).

3. RESULTS & DISCUSSION

3.1 Scaling Studies on Doped GeSb

To study the scaling limits of phase-change technology, doped GeSb was chosen as the phase-change material. Although GeSb is not a typical chalcogenide phase-change material, it was found that it forms a continuous flat film and possesses phase-change properties for films as thin as 1.3 nm [9]. Before making devices, basic material properties were measured on blanket films. Figure 3 shows results of the resistivity vs. temperature measurements (R-T curves) of thin films of doped GeSb and $Ge_2Sb_2Te_5$.

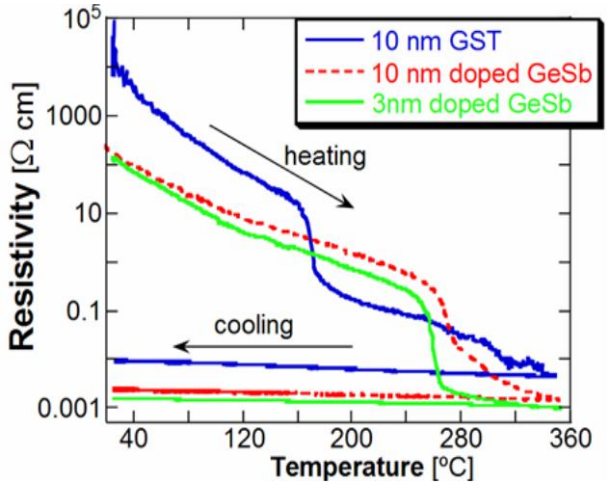

Fig. 3. Resistivity vs. Temperature (R-T) curves for $Ge_2Sb_2Te_5$ and doped GeSb with different thicknesses [6].

The crystallization temperature of doped GeSb is much higher than that of the $Ge_2Sb_2Te_5$ sample. The low resistance state of doped GeSb is less sensitive to temperature than that of $Ge_2Sb_2Te_5$. These results indicate that doped GeSb is a good candidate for phase-change memory.

Doped GeSb bridge devices were then made by the fabrication procedure introduced in the previous section. The length of the devices ranged from 40nm to 500 nm, with film thicknesses of either 3nm or 10 nm [6]. By using electron-beam lithography, the width of the device ranged from 20 nm to 200 nm. The smallest cross-sectional area of a functional device was only 60 nm^2. The current vs. voltage (I-V) curve is an important experiment for identifying operation feasibility of the devices. The "snapback" characteristic of the I-V curve above the threshold voltage ensures the power density sufficient for RESET (melting and quenching) of the device at low applied voltages. The apparent threshold voltage also helps separate the operation windows for read and write. The I-V curve of a doped GeSb device with snapback is shown in Fig. 4. The low threshold voltage of about 1V, corresponding to a threshold field of E=0.2 MV/cm, is also an advantage for building advanced devices.

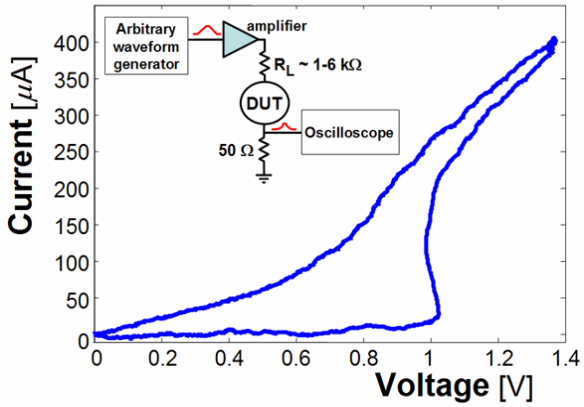

Fig.4. A typical current-voltage characteristic (I-V curve) for a phase-change bridge device with a film thickness of H=3nm, a width of W=50nm, and a length of L=50nm [6].

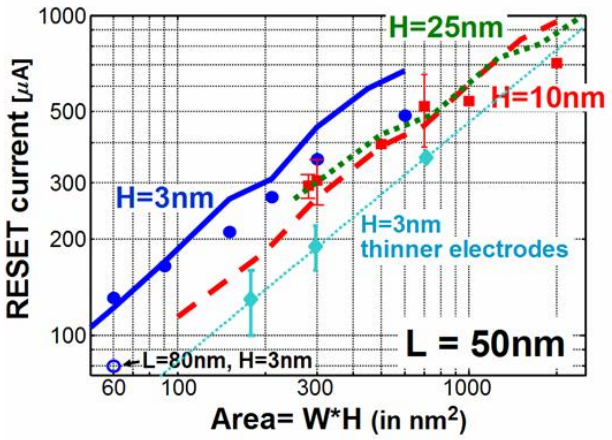

Fig. 5. RESET current of doped-GeSb phase-change bridge devices vs. the cross-sectional area defined by the lithographic bridge width W and the ultra-thin film thickness H [6].

The experimentally measured scaling of the RESET current is shown as dots in Fig. 5, and compared to predictions of numerical simulations (lines) [6]. The RESET current decreases as the cross-sectional area decreases. This result indicates that we can reduce the RESET current by reducing the film thickness, the width, or both. A hollow dot in the figure shows the lowest measured RESET current, obtained with a device with a length of 80 nm. A longer length can reduce the current because the heat is confined better when the thermally-conducting electrodes are further away from

the heating zone. Similarly, the RESET current of short phase-change bridges can be further reduced by increasing the thermal resistance of the electrodes. Measurements on phase-change bridge devices with thin (5 nm) electrodes of TaN rather than TiN showed a 40% improvement, mainly due to improving the thermal environment around the bridge [9]. In addition to the programming current, the programming speed of the doped-GeSb devices was investigated, indicating that both the RESET and SET operations could be performed with pulses shorter than 100 ns. With proper refinement, the RESET/SET speed can be reduced to 40ns [10].

Another important specification of solid-state memory is the cycling endurance. Figure 6 shows endurance of more than 10,000 SET-RESET cycles. Even though the device is highly scaled, this result already meets the lowest requirement for a NOR Flash memory. With further improvements on the material and the structure, an endurance of more than 100,000 cycles can be expected.

These studies on doped-GeSb reveal that the phase-change bridge structure is an excellent vehicle for scaling studies. The thickness of the thin film can be scaled in a well-controlled manner, and the flatness of the bottom electrode plays an important role for implementing ultra thin films and providing a good platform for further lithography steps.

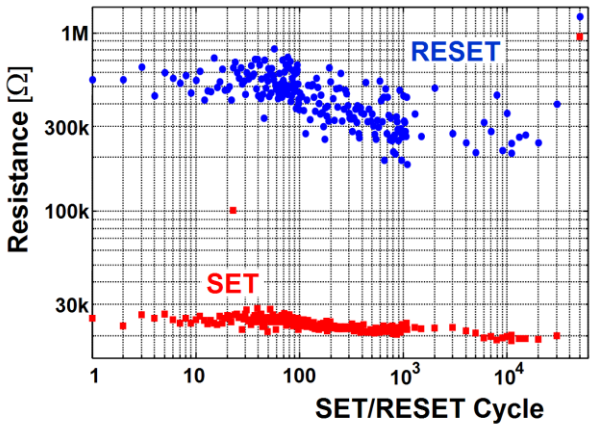

Fig. 6. Cycling endurance test of a doped GeSb phase-change bridge device [6].

3.2 New materials

Beyond the scaling study of Ref. [6], the phase-change bridge device also provides a vehicle for exploring new materials, such as undoped GeSb. Devices with a width of 40nm and thickness of 30nm were studied. Repeated RESET/SET tests could be performed (Fig. 7) with 10 ns pulses, indicating the possibility for ultra-high speed operation.

The research group from NXP also used bridge devices to investigate the Thomson effect [5]. They found that the carriers in the phase-change material (doped SbTe) carry a significant portion of the heat, shifting the heating profile of the device and producing asymmetric heating and crystallization profiles [5]. With careful design of the bridge geometry, they were able to reduce the RESET current by about 10% [5].

In addition to growth-dominated materials such as doped GeSb, GeSb, and SbTe, we are also interested in nucleation-dominated materials such as $Ge_2Sb_2Te_5$. A doped $Ge_2Sb_2Te_5$ phase-changed bridge device was also made by the same fabrication technique described in Section 2. The thickness of $Ge_2Sb_2Te_5$ was 5nm, the bridge width ranged from 20nm to 50nm, and the length ranged from 40 nm to 500 nm. For these devices, the new tester we describe in Section 3.3 was developed, in order to allow arbitrary waveforms and detailed investigation of the devices.

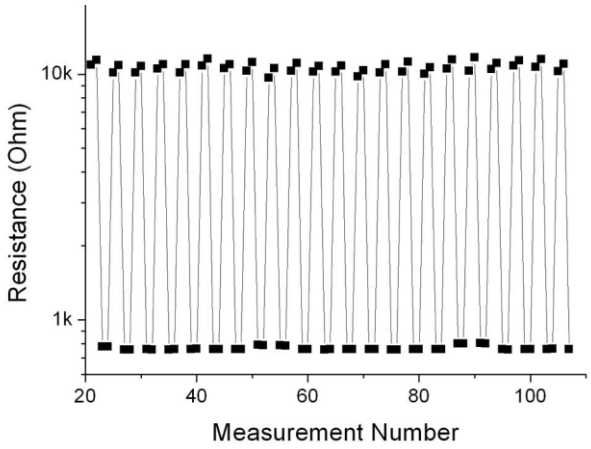

Fig. 7. SET-RESET cycling of undoped GeSb phase-change memory devices.

Phase-change bridge devices with doped $Ge_2Sb_2Te_5$ were evaluated with different types of pulses. While short RESET pulses can still be used with nucleation-dominated materials (Fig. 8(a)), significantly longer SET pulses are required. Square and trapezoid type pulses were used in this case (Fig. 8(b), (c)). The square pulses gave a uniform heating condition with accurate time control, so that we can use them to evaluate the SET speed of the device. The trapezoidal pulse was used for better control of the final resistance [12]. The devices were programmed to high resistance state (~10 Mohm) before every SET test and then were SET by different pulses. With square pulses, the $Ge_2Sb_2Te_5$ devices required pulses of about 700 ns to SET the device to R~100 kOhm. With trapezoidal pulses, the SET time could be reduced to about 100 ns. As shown in Ref. [12], the profile of the programming pulses clearly plays an important role in the final SET resistance of the devices.

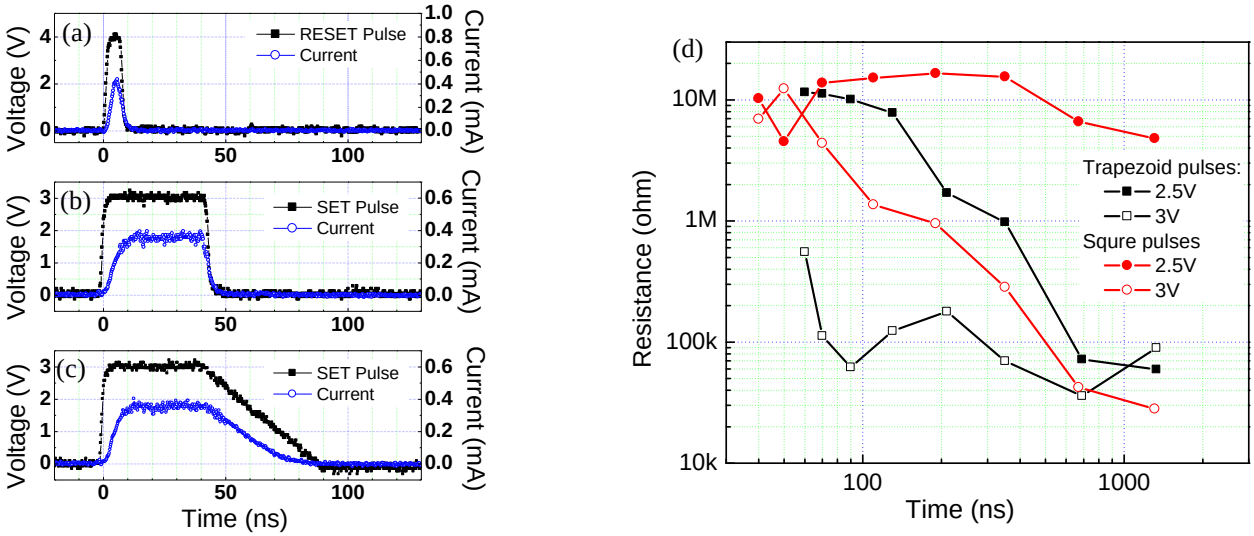

Fig. 8. Current and voltage traces of (a) a RESET pulse, (b) a square SET pulse, and (c) a trapezoid SET pulse. (d) Resistance of the device after SET pulses with variable pulse widths.

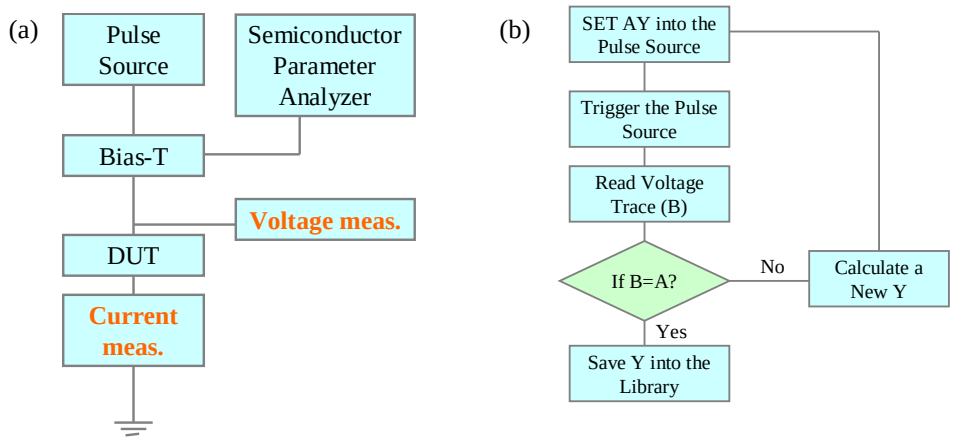

Fig. 9. (a) Layout of the testing setup, (b) The flow chart for compensating the system's distortion.

3.3 Testing improvements

Figure 9(a) shows the layout of the improved tester we have developed. The pulse source is an arbitrary waveform generator followed by an amplifier. A semiconductor parameter analyzer is used for accurate DC (direct current) resistance measurements. Bias-T indicates the switch for connecting DUT (device under test) with either the low frequency (or DC) measurement current from the semiconductor parameter analyzer or the high frequency pulse from the pulse source. We measure the voltage before the DUT and the current after the DUT using a digital oscilloscope. The voltage measurement used the high impedance mode (1 Mohm) while the current measurement used the low impedance mode (50 ohm). This tester setup can provide high voltage pulses (>10V) from a relatively low power pulse source along with an acceptable response time (~2.5ns). The high resistance state can also be measured accurately in this system. The most significant drawback of this tester layout is that the impedance of the DUT is typically not compatible with the pulse source, leading to significant reflections for uncorrected pulses.

In order to reduce the effect of these reflections and other system distortions, we used a computer-assisted feedback algorithm to trim the pulse profiles. If we consider the desired pulse we designed as A, the pulse that actually arrives at the device under test as B, and the undesired distortions of the system as X, then the relationship of A, B , and X is:

$$A X = B \qquad (1)$$

We introduce another matrix Y to compensate the distortion of the system X, so that

$$A Y X = B \qquad (2)$$

We can use the flowchart shown in Fig. 9(b) to gradually obtain an actual pulse at the DUT, B, that is very close to the desired pulse A.

A sample pulse shape result using a resistor as DUT is shown in Fig. 10. The pulse width is ~6ns in total with a ~3.5 ns FWHM (full width at half maximum). Although the resistor has a resistance of 2.7 kohm, there is no significant abnormal signal seen on either the current or the voltage trace. With this reliable testing system, we can fully explore the characteristics of high-speed devices.

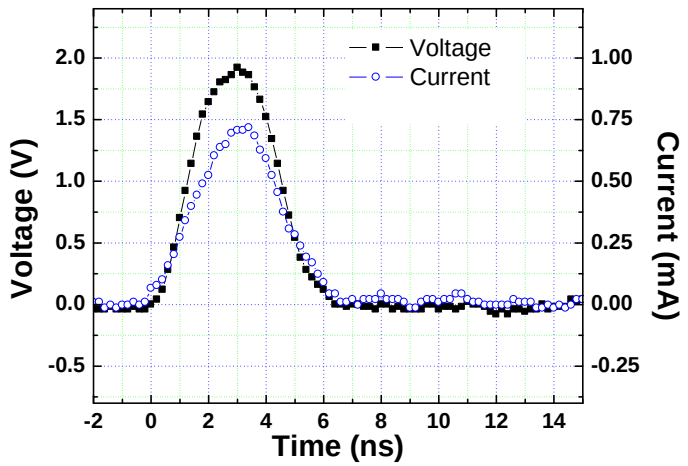

Fig. 10. A current trace and a voltage trace of a corrected pulse applied to a 2.7kOhm resistor.

4. CONCLUSION

In this work, we review the fabrication and application of phase-change bridge devices. The bridge device is a good vehicle for scaling studies, not only because the accurate control of the thickness relieves the pressure on lithography, but because the lithographic patterning of the bridge process is very similar to conventional gate patterning, which usually scales at 50% of the node feature-size in CMOS technology. The bridge structure was used to successfully demonstrate the scalability of phase-change memory down to 3 nm x20 nm cross-sectional dimensions. Furthermore, new materials can also be studied using the bridge structure since it offers a straightforward flat surface for material deposition, simplifying the achievement of good electrical contact. Several materials were evaluated with this structure. We also discussed testing of the devices and demonstrated the effect of the pulse profile on the SET speed for $Ge_2Sb_2Te_5$ devices.

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Biographies

Yi-Chou Chen received his B.S. degree and Ph.D. degree in Chemical Engineering in 1995 and 2000, respectively, both from National Taiwan University. In 2000, he joined Macronix International Co., Ltd. and worked on technology development of lithography, moving to the Emerging Central Lab in 2001 where he started working on phase-change memory. From 2005 to 2007, he was on assignment at the IBM Almaden Research Center. His current research interests include both phase-change materials and emerging memory devices. He is now a deputy department manager at Macronix.