Current Reduction in Ovonic Memory Devices

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ABSTRACT

Modern phase change memory devices require low programming currents to minimize cell size. Small cell size translates directly to commercial viability for OUM, where cell addressing can be accomplished by an MOS transistor. In sharp contrast to the original Ovonic memory devices which required many milliamperes and milliseconds to program, the modern Ovonic phase change material, now known as 225 GST, is orders of magnitude faster. The main challenge for a commercially viable memory was to reduce the programming current. The development of such a device started out with simple patterned metal/chalcogenide/metal sandwiched devices, which, though fast, required over one hundred milliamps of current to program to the amorphous state. Current reduction became the major priority for this modern phase change memory program and came about with a better understanding of programming dynamics, which were strongly coupled to the thermal environment of the device. Reduced heat losses through contacts, improved insulation around the device, and active heating significantly reduced the programming currents. Coupled with contact area reduction, E-beam and sublithographic devices routinely show programming currents below 1 mA. More recently, another means of current reduction was accomplished by reduction of the programmed volume for the same contact area.

Key words: phase change, Ovonic, non-volatile memory, 225 GST

1. INTRODUCTION

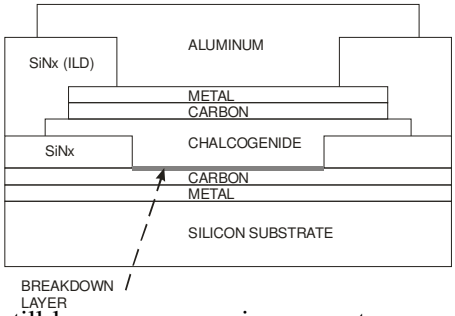
Devices based on phase change materials are the leading contender to replace today's flash memory. These unique, chalcogenide based materials, were invented by S. R. Ovshinsky about 40 years ago. [1,2] Their unique properties include electronic switching in the amorphous phase, a very large resistance change accompanying the phase change, a semiconductor-type activation energy, and radiation hardness to name a few. In 1999, T. Lowrey, Ward Parkinson, and Energy Conversion Devices (ECD) founded Ovonyx Inc. to pursue commercialization of chalcogenide based devices. [3] Soon after, BAE obtained a license to pursue development of chalcogenide based memories for radiation hard space applications. [4] And, shortly after that, Intel [5,6] licensed with and invested in Ovonyx. This was later followed by STMicroelectronics [7] in 2000. In 2005, Elpida Memory and Samsung licensed with Ovonyx to commercialize Ovonic Universal Memory (OUM) products.

Early memory devices made by Energy Conversion Device (ECD) were based on chalcogenide materials and relied on Te diffusion into (and out of) a region to form a highly conductive (resistive) matrix. [2] And although based on a slow segregation process, found an application in what was called an RMM (read mostly memory). [8] Material research, primarily in the optical rotating memory field led to improved materials [9] which did not rely on segregation but rather on "congruent" crystal nucleation and growth and formed the basis of re-writeable optical disks.

Based on a 1990 SBIR proposal titled "Non-Volatile Radiation Hard Memory using Ovonic Memory Switches" [10], the first modern OUM devices were fabricated in early 1990 as a proof of concept. These devices were based on what is now known as GST225, they were large in diameter (several microns), and they had metallic contacts on both sides. After numerous attempts and failures to program these devices, Mr. Ovshinsky suggested using faster, sub-microsecond pulse widths and the first modern OUM devices were born. However, they required large currents of about 150mA to reset. Further investigation, in particular the addition of carbon to the contacts, as well as thinner metals reduced the programming currents to several tens of milliamps.

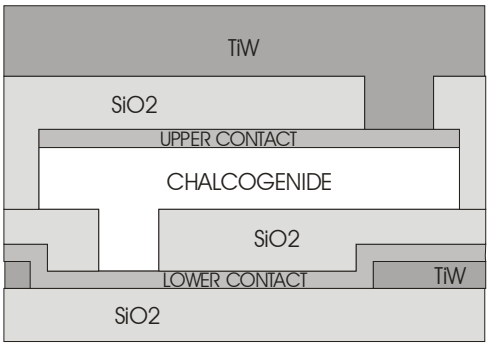
Breakdown devices The next major step in current reduction came with the discovery of breakdown layers. With 3 micron lithography, it was not possible for ECD to fabricate the needed small contact area devices for low programming currents. However, by controllably introducing an insulating layer over the lower contact, it became possible to produce large devices which behaved like small devices. These devices worked by an electronic breakdown of the thin, approximately 30A insulating layer, with a fairly small breakdown voltage of about 3 volts, forming a local hot spot where the current was focused and was able to locally heat the adjacent chalcogenide region to invoke phase change. Figure 1 is a schematic of a breakdown device as processed at ECD in the mid 90's. Among some of its attributes are relatively low programming currents of several milliamps as well as high dynamic range greater than 100x and very long cycle life, greater than 10^13 cycles.

Figure 1. Schematic of breakdown device



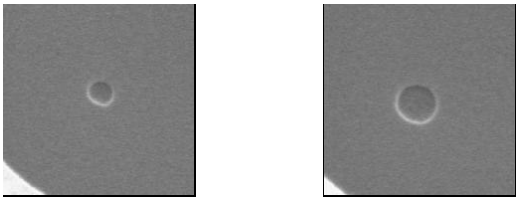
Insulated offset pore devices The need for still lower programming currents was apparent and research continued into reducing heat losses. Figure 2 shows the end result of optimizing ECD's planar process and was called the offset pore device. The offset was needed to minimize heat loss vertically from the device while maintaining low contact resistance to the device. The lower TiW was a strap to the actual lower device electrode contact which used various materials that varied in both thickness and resistivity to lower programming current by providing added heat and minimizing heat loss. The device top contact was also a thin film resistive layer to minimize device heat loss out of the top contact.

Figure 2. Schematic of insulated offset pore device



Despite all of these improvements, current reduction was slow in coming because the pore itself was still large. Therefore research was directed toward the reduction of pore size. This was accomplished with a collaborative effort with the University of Michigan. The University of Michigan had a converted SEM capable of writing in photoresist with an electron beam, thus being able to define very small pores. Figure 3 shows several SEM pictures of an 800Å and a 1600Å pore printed in SiNx.

Figure 3. SEM photos of submicron pores produced at the University of Michigan



Devices built on these E-beam defined features produced the first sub-milliamp devices. Figure 4 shows the RI and IV of an 800Å pore device. The reset current was approximately 200uA. A range of different size devices was produced and their reset currents measured and plotted in Figure 5. The reset current density for all these devices was about 2.5e6 A/cm2.

Figure 4. RI and IV curves of 800Å E-beam device

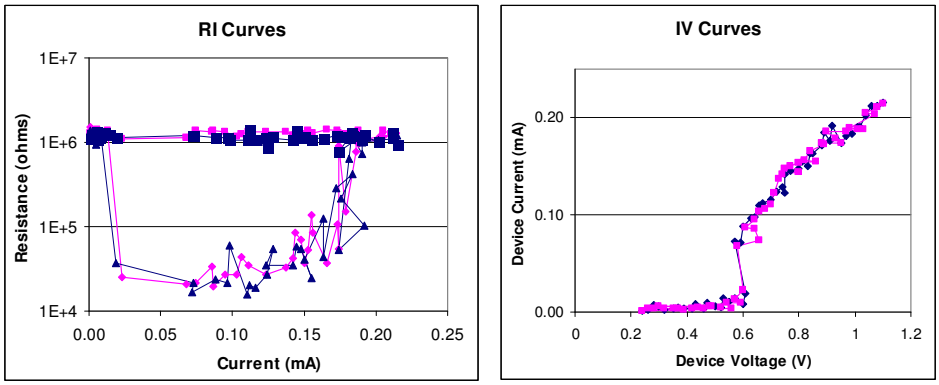
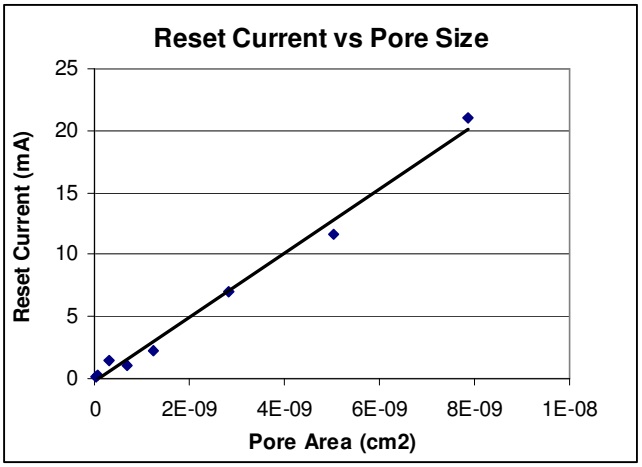


Figure 5 Current scaling of E-beam devices



2. EXPERIMENTS

Recently, experiments to reduce programming currents were carried out on base wafers from Elpida Memory, Inc. using several different approaches. The first investigation consisted of reducing the lower contact area to define a smaller device. Then local proximity Joule heating was added and heat loss was minimized to lower the programming current still further. Finally, programmed volume reduction was applied to minimize the programming current even further.

3. RESULTS & DISCUSSION

The first approach to reduce programming current was to reduce the lower contact area. Figure 6 is an SEM photograph of an Elpida base wafer showing three different device contact sizes which were used throughout this study. The respective pore sizes are around 660Å, 1080Å and 1560Å. These contacts are approximately level with the surface of the wafer after CMP planarization. The next figure, Figure 7, shows a typical cross-section of these devices.

Figure 6 SEM of an Elpida Memory base wafer

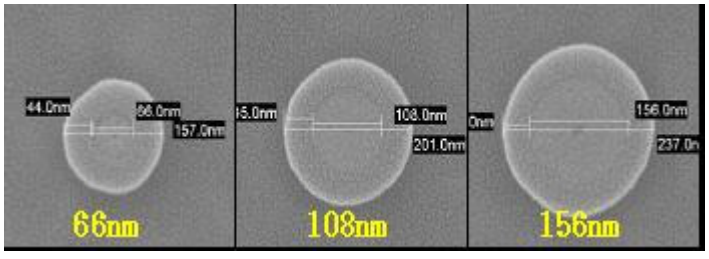
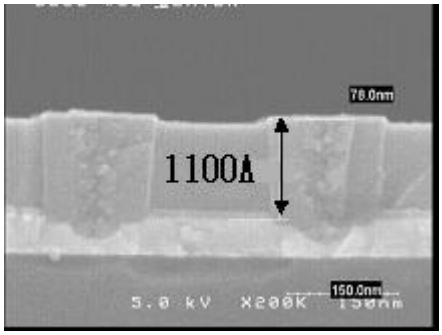
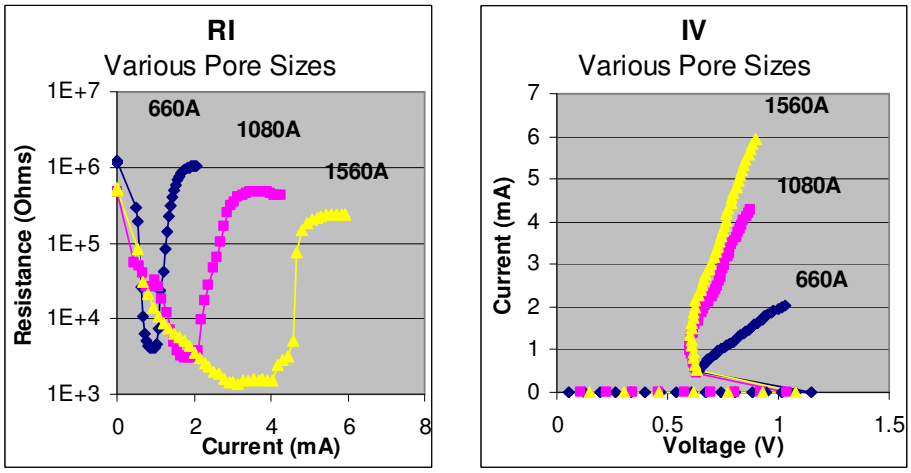


Figure 7 Cross section of an Elpida Memory base wafer



Device data taken on devices fabricated on these base wafers is shown in Figure 8 for the three nominal sizes for a fairly conductive lower contact material, TiN with a resistivity of 0.22 mOhm-cm. It is quite clear from the figures that as the pore size is reduced, the programming current is also reduced.

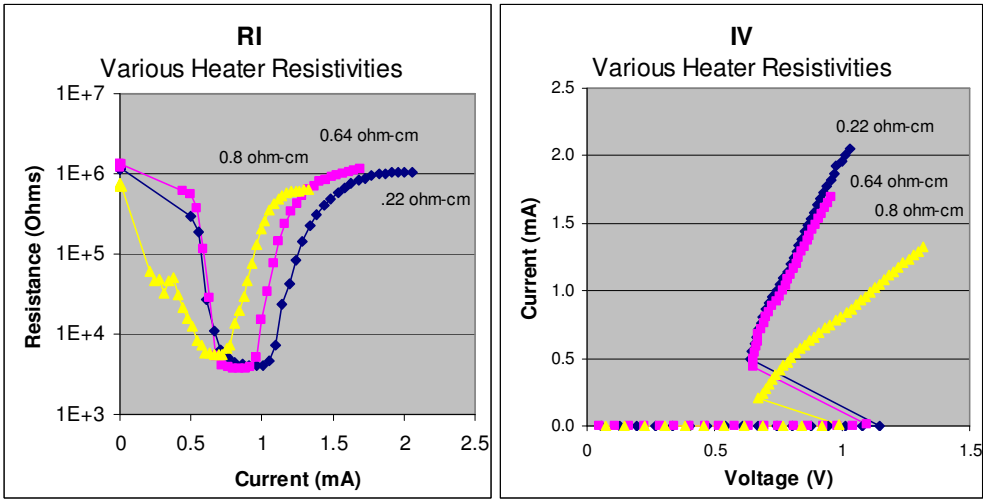
Figure 8. RIs and IVs of devices with different size lower contacts



Reducing programming volume can be pursued through the use of advanced lithographic capabilities to provide a reproducible minimum feature size. Pushing programming volume reduction by sublithographic techniques such as spacer formation, however, introduces excessive variability in the programming volume which is not desirable for volume manufacturing. Therefore, other means were investigated to lower the programming current still further.

Besides the chalcogenide device itself, the lower contact is the most critical to good device operation, since it is in intimate contact with the active region. In particular, its thermal properties directly affect the programming current. And, since heat is needed to raise the device temperature to the melting point, heat generation in the lower contact helps program the devices by providing additional joule heating to help induce a change of phase. The lower contact heater must generate as much heat as possible while minimizing the heat loss through the lower contact. This was accomplished by Elpida Memory by increasing the electrical and thermal resistivity of the heater. Increased electrical resistivity increases local heating and helps minimize heat loss, since the thermal conductivity is tied to electrical conductivity by the Wiedemann-Franz relationship. This means of reducing current is not as efficient as contact reduction, since some of the heat is generated outside and away from the programmed volume. Nonetheless, the reduction in programming current is very real. The price is an increased voltage drop as seen by an increase in the dV/dI (dynamic on resistance) of the device. This voltage drop can increase the on-chip voltage requirements and reduce the voltage margin available to program the device. Thus a compromise must be established in order to minimize the voltage drop and maximize the device efficiency. Figure 9 shows the results of increasing the resistivity of the heater from 0.22 mOhm-cm to 0.64 mOhm-cm to 0.8 mOhm-cm, where the current is reduced from over 1.5mA to about 1mA for the same structure shown previously. The IV curves show the increase in dV/dI as the resistivity is increased.

Figure 9. RIs and IVs of devices with varying lower contact resistivities



By increasing the resistivity still further, to several milliohm-cm, the current can be further reduced to almost 0.7mA for the smallest 660Å device as shown in Figure 10. Additional, but smaller improvements can be made by minimizing the heat loss through the lower contact still further, as shown in Figure 10 where the resistivity of the metalized layer below the heater is also increased to minimize the heat loss still further and the programming current drops to approximately 0.5mA.

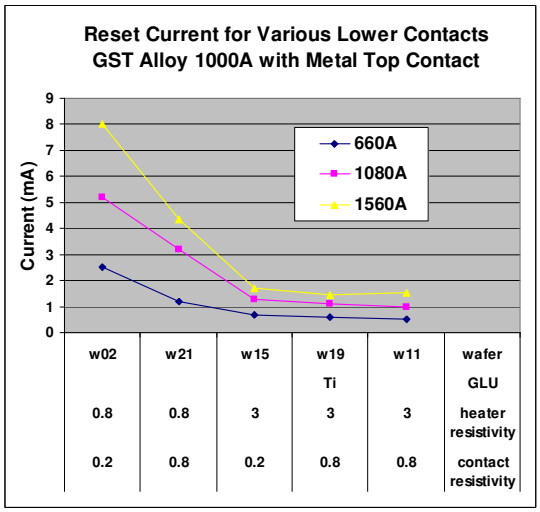


Figure 10. Current reduction with increased heater and lower contact resistivities

Another direct and more effective means of reducing programming current comes from actual reduction of the programmed volume [11]. Since a percolation path is all that is needed to create a fairly low resistance in a device, it stands to reason that only the amount of material making up this percolation path, about 20% of the GST, is needed for a large resistance change between amorphous (reset) and crystalline (set) states. The remainder of the material is used by the device to lower the resistance further by growing more crystals as well as increasing their size. But this needs more energy, so the current and/or time must be larger. This alone might not be so bad, except that this also means that the reset current must be larger to melt a larger volume. If part of the programming volume (which is beyond the percolation limit) were to be replaced by a totally inert non-conductive material, then not only would it not crystallize, but it would minimize lateral heat loss and help keep the grains from growing large and thus reduce the programming current. [12,13] We refer to these type of materials as composite GST alloys.

Composite GST alloys have been investigated by Ovonyx as a means of current reduction. As expected, the resistivity of the composite alloys is higher compared to GST. Also, there is a "useful" range, beyond which devices have problems setting. Figure 11 shows GST resistivity rising as the percentage of SiOx co-sputtered with the GST is increased.

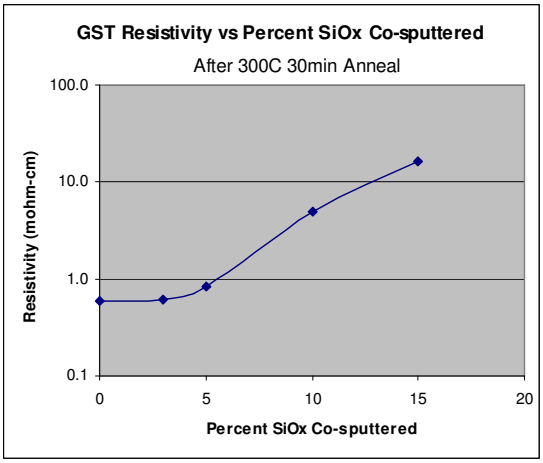


Figure 11. Composite GST resistivity verses percentage co-sputtered SiOx.

Key results from our investigation are summarized in the following figures. First, Figure 12 shows R-Is and I-Vs for devices made with various amounts of SiOx co-sputtered in GST alloys. As can be seen from the R-I curves, the programming current decreases as the amount of SiOx approaches 10% and then starts to saturate, as shown in Figure 13.

Figure 12 RIs and IVs for varying co-sputtered percentages with GST.

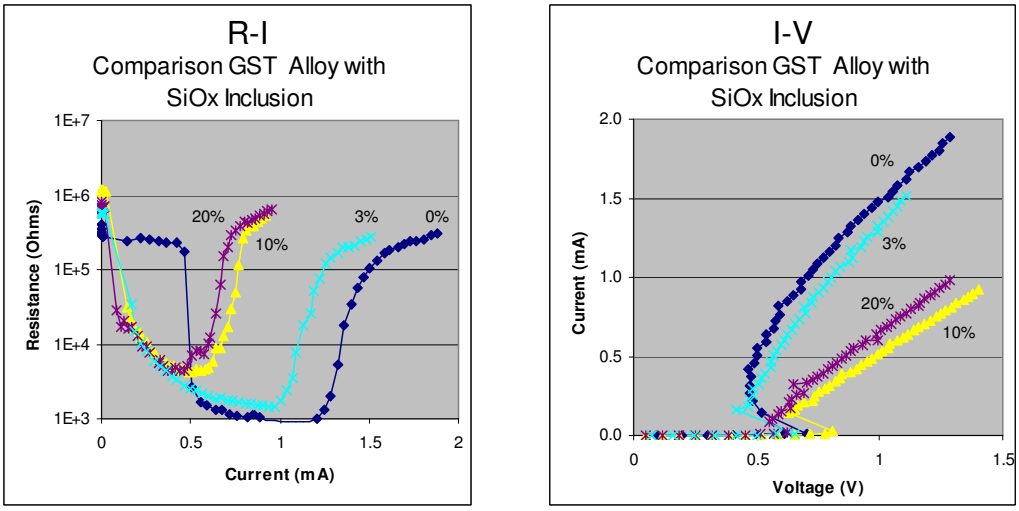
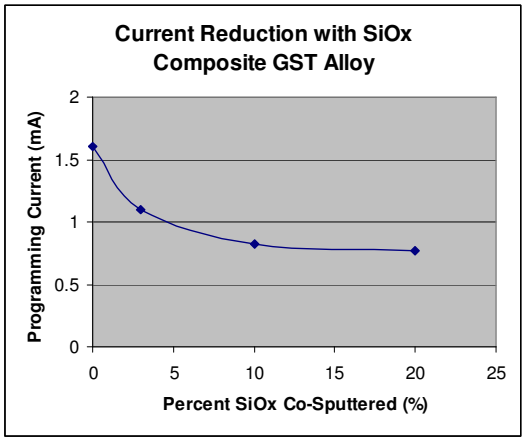
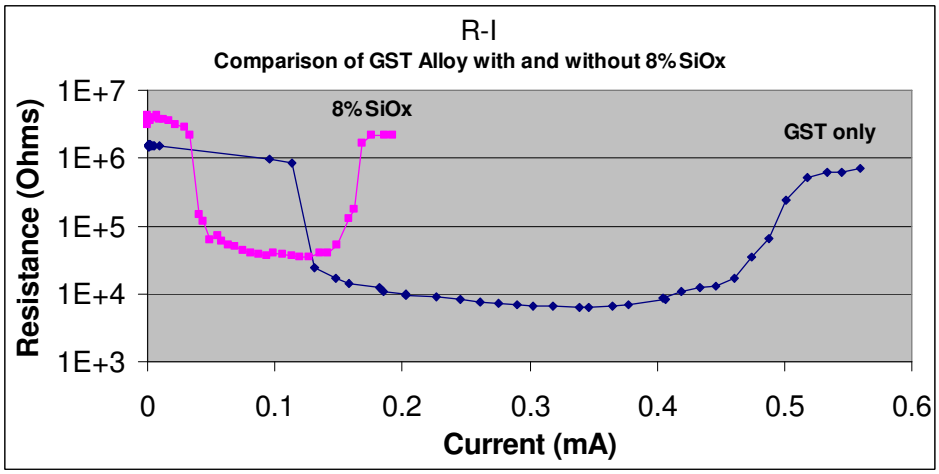


Figure 13 Programming current reduction for varying co-sputtered percentages with GST.



Finally, Figure 14 shows RI curves for devices fabricated by employing all of the current reducing measures compared to a reference, GST only device. For the smallest pore devices, with the optimized base heater, and with SiOx inclusion in the GST alloy, we have been able to reduce programming current to less than 200uA. Figure 15 shows the device's IV curves.

Figure 14 RIs for 0% and 8% SiOx co-sputtered with GST device on optimized base.



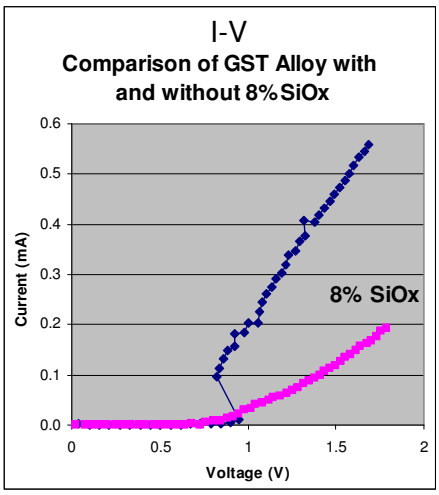


Figure 15 IVs for 0% and 8% SiOx co-sputtered with GST device on optimized base.

Other composite GST alloys have also been investigated and also show current reduction. Table 1 contains some of these composite alloys, the range investigated and the approximate observed current reduction.

Compound	Range investigated (%)	Ireset Reduction (%)
GST Control		0
SiOx	3 to 30	65
SiNx	5 to 20	50
C	5 to 20	40
SiC	5 to 20	50

Table 1 Composite materials investigated with approximate current reduction.

4. CONCLUSION

Current reduction in Ovonic memory devices has proceeded quite dramatically. Starting with 100's of milliamps in big devices with metallic contacts, to several milliamps in reduced contact area devices with insulation, to less than 200 microamperes in heated, insulated, reduced area and reduced volume devices. Having reduced the programming currents to MOS device levels, the next challenges come from mass production of these devices for various applications.

4. ACKNOWLEDGEMENTS

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Biographies

Wally Czubatyj, [59], Director of Engineering – Ovonyx Technologies, Inc.

Wally Czubatyj was born in Germany in 1946. He got his PhD in Electrical Engineering from Wayne State University in 1977 and started his professional career at Energy Conversion Devices. As a research scientist, he pursued his interests in thin films, photovoltaics and chalcogenides with emphasis on microelectronic devices. After several years as a research scientist he became the program manager and then the director of the microelectronics group, where he was able to pursue novel device development. In the mid to late 80s, his interests changed from amorphous silicon for solar cell and display applications to chalcogenides for microelectronic applications in the switching and memory areas. His 1989 proposal to investigate devices based on new congruent crystallizing chalcogenide materials for radiation hard non-volatile memory applications renewed interest in the electronic chalcogenide memory program where he has worked ever since. During the 1990's he led the effort at ECD to reduce the programming current in chalcogenide based memory devices and in 1999 he joined Ovonyx Inc. to pursue commercialization of these devices. At OTI he continues to research memory devices and materials as well as work toward development and commercialization of non-volatile memory products. He currently has 22 issued patents, 7 applied for and others pending.

Tyler Lowrey, [52], President, Chief Executive Officer and Director – Ovonyx, Inc.

Mr. Lowrey has overall responsibility for the Company and its projects, alliances, outside investors, investments and day-to-day operations. The Company is chartered with commercializing chalcogenide phase-change nonvolatile memory devices that the Company calls Ovonic Unified Memory ("OUM"). He is the inventor/co-inventor of more than 100 U.S. patents related to semiconductor memories and more than 30 OUM-related patent disclosures. Mr. Lowrey has an extensive background in solid-state IC memories and their development, debug and ramp-up to high-volume competitive production. He served as a process engineer and device engineer and in mid-level and senior-level management positions at Micron Technology, a Fortune 500 memory producer. While at Micron, he was Vice President-Chief Technical Officer and Vice President-Chief Operating Officer as well as a director and Vice Chairman of Micron's board of directors. As part of the Company's joint development programs with the Company's licensees, Mr. Lowrey assists to evaluate, debug and optimize the processes, materials, devices and cell structures – with particular attention to processes and electrical characterizations. Mr. Lowrey is presently on the Board of Directors of Litel Corp.

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1959-1965; Dnepropetrovsk University, Dnepropetrovsk, Ukraine. Research associate, Assistant professor. Flat solid-state image amplifier and TV-screen. Deposition of sublimed films of ZnS: Mn. Structure, electrical properties and electroluminescence of sublimed ZnS: Mn films. **1965-1966** Hull University, UK. Research Associate. The role of conductive inclusions in electroluminescent ZnS, ZnSe. **1966-1967** Dnepropetrovsk University, Ukraine, Associate Professor, Electroluminescence in Crystals and Thin-Films of II-VI Semiconductors. Intervalley scattering in GaAs. **1967-1991** Institute of Technical Mechanics of the Academy of Sciences of Ukraine, Dnepropetrovsk. Head of the Department of Semiconductor Electronics. Principal investigator for more than 20 projects in fundamental and applied physics of electronic instabilities in a media with a bulk N- and S-type Negative Differential Conductivity (NDC). **1970-1971** Virginia Polytechnic Institute and State University**,** VA, USA**,** Wayne State University, Detroit, MI, USA. Research Associate. Modes of switching in chalcogenide Ovonic Threshold Switch (OTS) and other materials; intervalley transfer in GaSb. **1991 -1999** Energy Conversion Devices, Inc., Troy, MI, USA, Senior Research Scientist; Development of Chalcogenide High-Speed Multistate Ovonic EEPROM. **1999 to present time** Ovonyx, Inc, Rochester Hills, MI, USA. Principal Research Scientist. Development and optimization of Ovonic Unified Memory (OUM) and OTS. Published (in co authorship) **3 books** (on electrical switching in amorphous semiconductors, on Gunn-effect devices and on interlayer interaction in multilayered structures with S- and N-type NDC), more than 200 papers and patents.

Isamu Asano …was born in Nagoya,Japan in 1959. He received B.S.(1982) and M.S.(1985) from Nagoya University in Material Engineering and Ph.D. in Electrical Engineering from Tohoku University in 2002. In 1985 he joined Device Development Center / Hitachi Ltd. and had worked for development process and materials for leading edge DRAMs. He also had his research activity as a visiting scholar in Center for Integrated Systems / Stanford University from 1991 to 1992 to study Cu-CVD systems. In 1992 he joined preliminary development team of Ta_2O_5 capacitor in 16Mbit DRAM application and reported its achievement in IEDM/1996. Mr.Asano has moved to Elpida Memory Inc. from 2000. Since 2003 he has been in charge of development project as manager for commercializing High Speed Phase-change Random Access Memory.