Program window of doped Sb_2Te phase change line cells

Friso J. Jedema [a], Micha A.A. in 't Zandt [a], Rob A.M. Wolters [a], Romain Delhougne [b], Dirk J. Gravesteijn [b], David Tio Castro [b], G.A.M Hurkx [b] and K. Attenborough [b]

[a] NXP Semiconductors, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands, friso.jedema@nxp.com
[b] NXP Semiconductors, Kapeldreef 75, 3001 Leuven, Belgium

ABSTRACT

A promising candidate for a scalable non-volatile memory is Phase Change Random Access Memory. Recently, we have demonstrated the feasibility of a novel PCRAM memory cell concept based on a narrow line of a doped-Sb_2Te phase-change material[1]. In this paper the programming window of doped-Sb_2Te line cells will be addressed, for which two properties are most important. The first property is the reset current to program the line cell into the amorphous reset state. A low reset current is desired in order to minimize the size of the select transistor and hence the memory cell size. It is shown that the magnitude of the reset current of doped-Sb_2Te line cells scales linearly with the line width. A minimum reset current of 550 μA is obtained for 25 nm wide lines. The second property concerns the threshold voltage, the magnitude of which should preferably be below the available on-chip supply voltage for embedded applications. The magnitude of the threshold voltage is observed to be dependent on the amorphous line resistance, amorphous line length and delay time between a reset and set pulse. The threshold switching event self occurs in a very short time frame, typically less than 1 ns.

Key words: PCRAM, line cell, doped Sb_2Te, reset current, threshold voltage

1. INTRODUCTION

At present, the technology of choice for non-volatile memory in integrated circuits is Flash technology. However, it is foreseen that this technology will not continue to scale sufficiently in the near future. Phase change random access memory (PCRAM) is expected to become the main stream technology to replace the Flash technology.[2] It offers better scalability, higher programming speeds, smaller cell sizes and less lithographic mask steps for manufacturing.

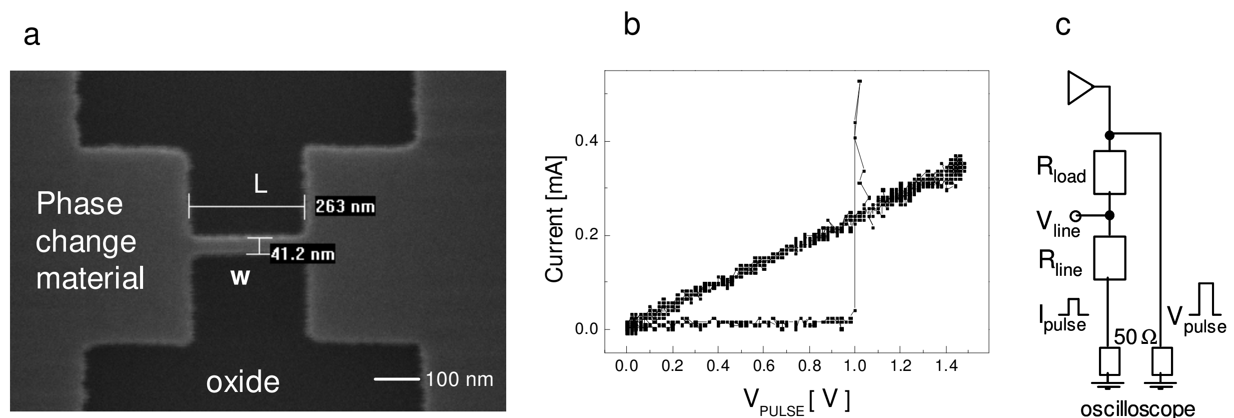

Figure 1 – (a) Top view scanning electron microscope picture of a PCRAM line cell with a (designed) width w= 50 nm and a length L= 250 nm. (b) Set pulse I-V characteristic of a 50-250 nm line cell with R_{LOAD} = 3 kΩ. The set pulse had a leading edge time of 100 ns, a 100 ns plateau and a falling edge time of 300 ns. (c) Schematic representation of the measurement circuit.

A PCRAM line cell can be programmed and erased by heating the line of phase change material with an electrical pulse. Programming involves first the melting of the phase change material, subsequently followed by a very short cooling time of a few nanoseconds. This enables the phase change material to solidify into an amorphous state, called the reset state. The resistance of the line in the reset state is about 3 orders of magnitude larger than the resistance in the crystalline set state. For erasing a programmed bit, the line of the phase change material is heated below the melting temperature, but above the crystallization temperature, for a duration of tens of nanoseconds. This enables the amorphous material to return from a reset state into the set state.

An example of a 50 nm wide and 250 nm long phase change line is shown in Fig. 1a. The line cell is fabricated on a (100) Si wafer with a 500 nm grown thermal oxide layer. First, 100 nm thick TiW bottom electrodes are deposited and patterned by standard optical lithography. Then a film of 20 nm phase change material (PCM) is sputter deposited and the line cells are subsequently patterned by e-beam lithography and Ar plasma etching. A typical I-V plot of a set pulse applied to a 50-250 nm line cell is shown in Fig. 1b, whereas the measurement circuit is shown in Fig. 1c. Note that the peaks in current pulses in Fig. 1b at the moment of switching are attributed to parasitic capacitances in the measurement circuit.[3] Without the 3 kΩ load resistor, the peaks in I-V's are absent.

2. RESET PROGRAMMING

In Fig. 2 a reset current sweep is shown for a 50-250 nm line cell. A reset sweep starts with a measurement of the initial crystalline resistance of R_{LINE}, typically around 1 kΩ. Here R_{LINE} is the resistance of the line measured between the bond pads. Subsequently, reset pulses of 50 ns duration with a leading edge and trailing edge of 4 ns are applied with increasing amplitude. After each reset pulse, the resistance is measured with a delay time of approximately 1 second. Once the sample is programmed into the amorphous reset state, the sample is brought back to its crystalline set state by applying a set pulse of 300 ns duration, having leading and trailing edges of 100 ns. A load resistor of 3 kΩ is included in the measurement circuit during the sweep, in order to limit the magnitude of the current after threshold switching has occurred in the set pulse.

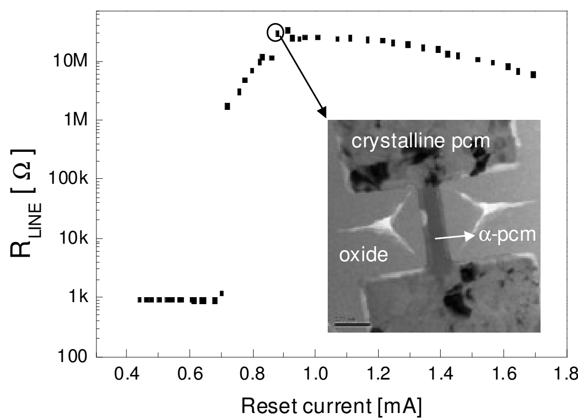

Figure 2 – Reset current sweep of a 50-250 nm line. R_{LOAD} = 3 kΩ. The insert shows a transmission electron microscopy picture of the line for a reset current of 0.9 mA. Note that the complete line is amorphised.

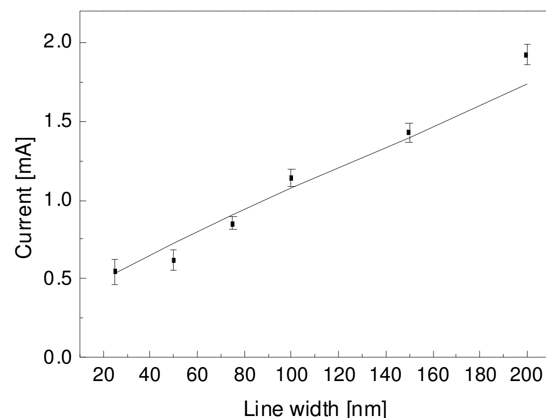

Figure 3 – Minimal reset current as a function of line width. The length for each line is 5 times its width, i.e. 5 squares long. Each data point represents an average of 4 to 6 samples. The solid line shows the simulation result.

Figure 2 shows that a minimal reset current of 700 μA is needed to program the 50-250 line into the amorphous reset state. From that point on, a continuous increase of the amorphous state resistance is observed with increasing reset currents. This is attributed to a continuously increasing size of the amorphous spot in the phase change line. A maximum in the reset state resistance is observed for a reset current of 0.9 mA. At this point transmission electron microscopy (TEM) images indicates that the line is fully amorphous, see insert in Fig. 2. A decrease in the reset state resistance of the line is observed when applying reset currents larger than 0.9 mA.

Figure 3 shows the minimal reset current to obtain the amorphous reset state as a function a line width. Each data point represents an average of 4 to 6 samples. A linear scaling is observed when the line width is reduced from 200 nm to 25 nm. Figure 3 shows that at a line width of 25 nm, a reset current of 550 μA is needed to program the line into the reset state. Extrapolation of the linear scaling to infinitesimal widths yields a finite offset current. This current physically represents the energy that is lost in heating the environment of the line. Note that for line widths smaller than 20 nm, a reduction of the thickness of the phase change layer will become more effective for reducing the reset current, than reducing its line width.[5]

Concluding, the above shows that the smallest obtainable reset current for 20 nm thick, 25 nm wide and 125 nm long phase change lines with doped Sb_2Te phase change material is 550 μA.

3. SET PROGRAMMING

During set programming, a large voltage for heating is avoided by a threshold switching event. For voltages smaller than the threshold voltage, a PCRAM line cell in the amorphous reset state does not conduct the required current to be programmed into the crystalline set state. An example of a set pulse showing a threshold switching event of a 50-250 nm PC line is shown in Fig. 1b. No detectable current is flowing in the reset state, until the voltage reaches the threshold voltage (V_T) at 1 Volt. At this point a rapid increase in the current occurs within 1 ns and the line switches into its crystalline set state.

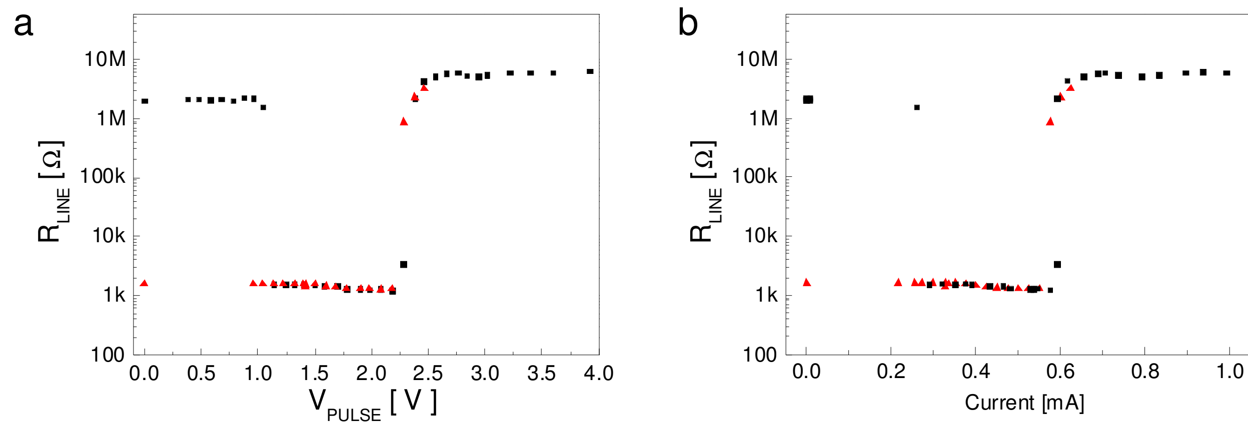

Figure 4 – Set program window of a 50-250 nm line cell, (a) as a function of pulse voltage and (b) as a function of pulse current. R_{LOAD} = 3 kΩ. The black squares represent the reset-to-set and reset-to-reset programming (set sweep), whereas the red triangles represent the set-to-reset programming (reset sweep) .

In Fig. 4 the program window is shown for a 50-250 nm line cell. A set sweep, indicated by the black squares in Fig. 4, starts by programming the 50-250 nm line cell into a reset state of R_{LINE} = 2 MΩ. Subsequently, 50 ns set pulses with increasing magnitude are applied to the line cell, starting from 0.3 Volt. Examples of several set pulses are shown in Fig. 8. After each pulse, the resistance of the line is measured. In case the measured resistance is larger than 1 MΩ, a set pulse with increased voltage is given, otherwise a reset pulse is given to bring the line back to the 2 MΩ reset state.

Figure 4a shows that for voltages below V_T = 1 Volt, the 50-250 nm line remains in the amorphous reset state. A pulse with a voltage of 1.1 Volt and a current of 0.3 mA enables the first transition from the reset to the set state. This shows that V_T is the limiting factor for reset to set programming. The required set current of 0.3 mA to establish the phase transition could be obtained at a lower pulse voltage of only ~ 0.3 Volt, in case the 3 kΩ load resistor would be absent. Increasing the set pulse voltage beyond 1.2 Volt shows a gradual reduction in the resistance of the set state, until reset to reset programming is obtained beyond 2.4 Volt, corresponding to a current of 0.6 mA as shown in Fig. 4b. For comparison a reset sweep has been included in Fig 4 as well, indicated by the red triangular points.

Concluding, the above shows that the smallest obtainable set voltage for a 50-250 nm line cell with a 2MΩ reset resistance is 1.1 Volt. The threshold voltage is shown to be the limiting factor for the set voltage.

4. THRESHOLD VOLTAGE DEPENDENCES

As the threshold voltage is determining minimum voltage at which the line cell can be programmed from the reset to the set state, it represents an essential property of the PCRAM line cell. Therefore its dependences on the amorphous reset resistance, amorphous line length and time are important.

In figure 5 the threshold voltage is plotted as a function of the reset resistance. Figure 5 shows that the magnitude of the threshold voltages increases with the reset resistance. This is to be expected as a higher resistance means that a larger part of the line is amorphised. At the largest amorphous reset resistance of 30 MΩ, programmed with a reset current of 0.9 mA, the threshold voltage is 3 Volt. This value represents the threshold voltage of a completely amorphised line, in this case with a length of 250 nm, as indicated by the TEM picture in the insert of Fig. 2. Interestingly, when larger reset currents than 0.9 mA are used, the amorphous rest resistance is decreasing, but the threshold voltage is increasing. This trend is indicated by the red triangular data points in Fig. 5. As the threshold voltage should be minimized for obtaining a proper set regime in the available voltage window, one should therefore avoid exposing the 50-250 nm line cell to higher reset currents than 900 μA.

By performing similar experiments for longer line lengths, one can obtain the threshold voltage as a function of line length. This is performed for line cells with lengths ranging from 100 nm to 400 nm and the result is plotted in Fig. 6. Applying a linear fit to the data points in Fig. 6 yields the following relation: $V_T = 8xL + 1$. Here V_T is the threshold voltage in Volts and L is the amorphous line length in μm. Note that this relation is valid for threshold voltages obtained at a time of approximately 1 second after a reset pulse has been given and is valid only for lines not programmed beyond there maximum reset state resistance, eg. $I_{reset} < 0.9$ mA for the 50-250 nm line in Fig. 2. Figure 6 shows the threshold voltage has a finite positive offset of about 1 ± 0.4 Volt. At present the origin of this offset is unclear. However, one explanation for the offset voltage could be that it is related to the band gap of the amorphous phase change material. The band gap represents the minimal energy a charge carrier has to acquire to be excited from the valence into the conduction band. This energy scale is relevant for the process of impact ionization, which is reported to be responsible for the threshold switching in GST 225 phase change materials.[6,7]

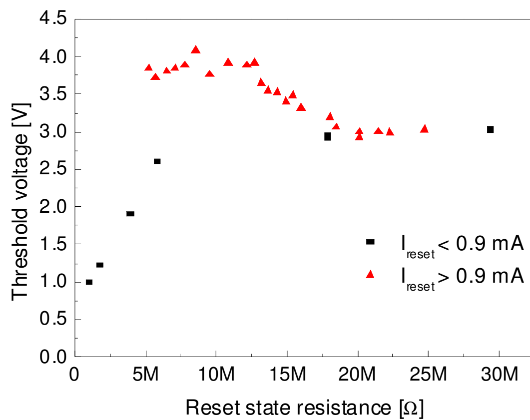

Figure 5 – Threshold voltage dependence of a 50-250 nm line cell, as a function of the amorphous reset state resistance. The black square data points correspond to amorphous reset state resistances obtained with a reset current < 0.9 mA, whereas the red triangular data points correspond to amorphous reset state resistances obtained with a reset current > 0.9 mA, see Fig. 2.

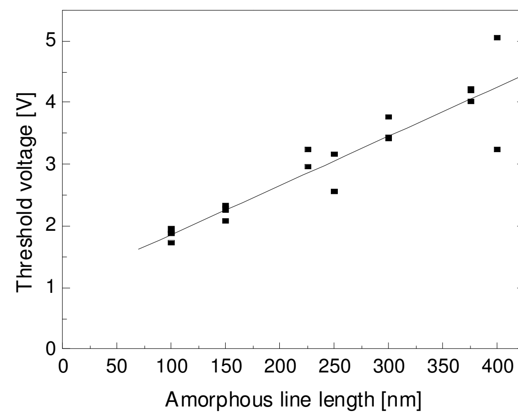

Figure 6 – Threshold voltage dependence, as a function of amorphous line length. The square data points indicate the threshold voltage for completely amorphised lines, as indicated by a maximum in the amorphous state resistance in reset current sweeps, similar to Fig. 2. The solid line represents a linear fit to the data points. Note that the threshold voltage was determined at approximately 1 second after a reset pulse was given.

The threshold voltage is also found to be dependent on the time between the reset pulse and the consecutive applied set pulse. An experiment with a series of reset-set pulses was carried out, having a variable delay time between the end of the reset pulse and the occurrence of a threshold switching event in the subsequent set pulse. In Fig. 7 the threshold voltage is plotted as a function of this reset-set delay time for a 75-300 nm line cell. The reset-set pulse had a 50 ns reset pulse with a reset current 0.8 mA, resulting in a 1 MΩ amorphous reset state. From Fig. 7 it can be observed that longer reset-set delay times lead to a monotonous increase in the magnitude of the threshold voltage. A similar behavior has also been observed for the GST 225 phase change material, and is reported to be caused by intrinsic trap dynamics in the amorphous state.[5] Figure 7 furthermore indicates that a line cell can be read out as quick as 50 ns after a reset pulse has been applied, provided that the read out voltage is less than 0.5 Volt. Note that only at shorter delay times than 1 second the magnitude of the threshold voltage is lower than the offset voltage as observed in Fig. 6. At a delay time of 1 second the threshold voltage is 0.9 Volt, in close agreement with the data shown in Fig. 5 and Fig.6 .

Another interesting observation is that the occurrence of a threshold switching event has a voltage dependent delay time.[8] Here the delay time is defined as the time in between the start of the set pulse, excluding the 4 ns rise time, and the occurrence of the threshold switching event. Figure 8 shows that a time delay is observed between the start of the voltage pulse and the occurrence of a threshold switching event. As the voltage amplitude increases, this delay time is reduced. This trend is shown in the bottom insert of Fig. 8. A monotonous decrease in the delay time is observed from 45 ns to 2 ns, when the set pulse voltage is increased from 1.1 Volt to 2.6 Volt.

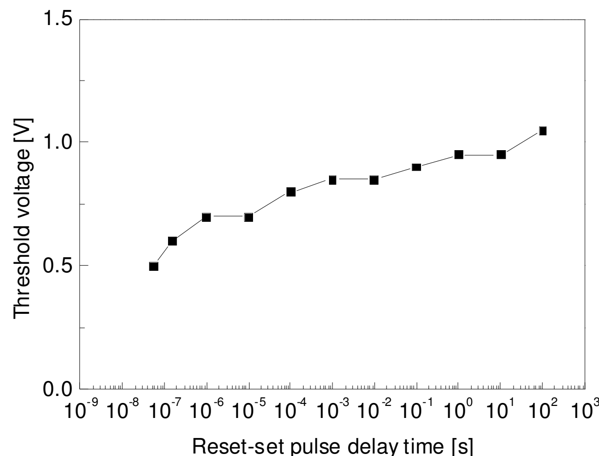

Figure 7– Threshold voltage dependence of a 75-300 nm line, as a function of reset-set delay time. The square points are the measured threshold voltages after applying a 50 ns reset pulse with an amplitude of 3.7 V and 0.8 mA. The set pulse had an amplitude of 3.7 V and 0.8 mA with a duration of 700 ns, having a 100 ns leading edge and a 500 ns trailing edge. The solid line serves as guide to the eye. R_{LOAD} = 3.3 kΩ.

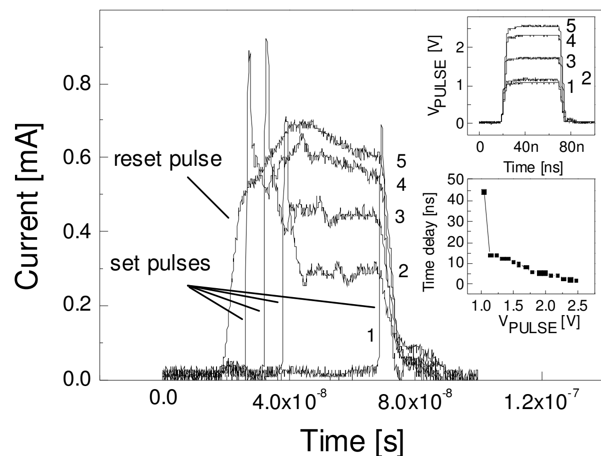

Figure 8– Threshold voltage switching event delay time as a function of the pulse voltage. The reset (5) and set pulses (1,2,3 and 4) are taken from the same set sweep as applied to the 50-250 nm line cell in Fig. 4. The reset state resistance prior to the set pulse was 2MΩ. Top right insert: the associated voltage waveforms. Lower right insert: delay time for the occurrence of a threshold switching event, as a function of V_{PULSE}. R_{LOAD} = 3 kΩ.

Concluding, the above shows that the threshold voltage is dependent on the amorphous reset state resistance, amorphous line length and time. Figures 5 till 7 show that the threshold voltage can be kept as low 1 Volt, which is below the on chip supply voltage for embedded memories at the 45 nm node.

5. CONCLUSION

The programming window of the PCRAM line concept with doped Sb_2Te material is measured. Reset currents as low as 550 µA are possible for 20 nm thick, 25 nm wide and 125 nm long phase change line cells. Secondly it is shown that the minimum set voltage is limited by the threshold voltage. The threshold voltage is dependent on the amorphous state resistance, amorphous line length and time, but can be kept below the available on chip supply voltage.

REFERENCES

1. M.H.R. Lankhorst, W.S.M.M. Ketelaars, R.A.M. Wolters, Nat. Mater. 4, 347-352 (2005).
2. A.L. Lacaita, Solid-State Electronics 50, 24-31 (2006)
3. S. Lai, Tech. Dig. - Int. Electron Devices Meet. 2003, 255
4. D. Ielmini, D. Mantegazza, A.L. Lacaita, A. Pirovano and F. Pellizer, IEEE Electron device letters , Vol. 26, No. 11 2005
5. Y.C. Chen et al., Int. Electron Devices Meet. 2006
6. D. Ielmini, A.L. Lacaita, and D. Mantegazza, IEEE Transactions on electron devices, Vol. 54, No. 2, February 2007
7. A. Pirovano, A.L. Lacaita, A. Benvenuti, F. Pellizzer and R. Bez, IEEE Transactions on electron devices, Vol. 51, No. 3, March 2004
8. S.R. Ovshinky and H. Fritzsche, IEEE Transactions on electron devices, Vol. 20, No. 2 (1973)

Acknowledgements

The authors would like to acknowledge M. Kaiser and M. Verheijen from the Materials Analysis department at Philips Research for their TEM work.

Biography

Friso Jedema was born in 1973. From 1991 to 1997 he studied Applied Physics at the Univerity of Twente, graduating on the subject of High T_C superconducting quantum interference devices. In 2002 he obtained his doctorate degree from the faculty of mathematical and physical Sciences at the Rijksuniversiteit Groningen. The subject of his thesis was spin polarized electron transport in metallic mesoscopic spin valves. The research was carried out in the group of prof. B.J. van Wees. In 2003 he started working in the optical storage sector at Philips Research. At present he is a senior scientist at NXP Semiconductors, working on phase change random access memories.