

Phase-Change Memory with Carbon Nanotube Electrodes

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ABSTRACT

We demonstrate control of phase-change memory (PCM) bits using carbon nanotubes (CNTs), which represent the ultimate limit of nanoscale electrodes. This configuration reduces PCM programming currents to $<5 \mu\text{A}$, about two orders of magnitude lower than present state-of-the-art. Memory switching with pulsed measurements show very low energy consumption ($\sim\text{fJ/bit}$), and excellent device scalability toward sub-Volt and sub- μA operation. We also report a novel technique to fabricate PCM nanowires self-aligned with their CNT electrodes, leading to further improvements in device performance.

Key words: GST, phase-change, low-power, carbon nanotube

1. INTRODUCTION

Phase change materials (PCMs) are typically chalcogenides like $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) which have amorphous (a) and crystalline (c) phases with contrasting electrical and optical properties. Electrically-programmable PCMs have captivated wide interest for applications in non-volatile memory¹ and reprogrammable circuits² with low voltage operation, fast access times, and high endurance. However, a drawback of PCMs is their high programming current ($>0.1 \text{ mA}$), as Joule heat must be coupled to a finite bit volume, previously achieved with 30-100 nm diameter nanowires³ or metal vias.⁴

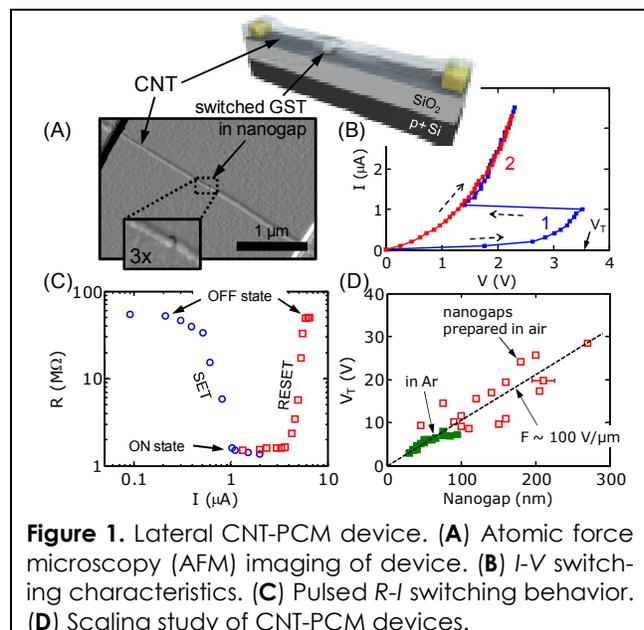
2. RESULTS & DISCUSSION

We used carbon nanotubes (CNTs) with diameters ~ 1 to 6 nm as electrodes^{1,5} to reversibly induce phase change in nanoscale GST bits. Our findings address the potential size and power reduction that are possible for programmable bits of PCM. We demonstrate reversible switching with programming currents typically $<5 \mu\text{A}$, two orders of magnitude lower than state-of-the-art PCM devices.

After fabricating CNT devices,^{1,5,6} we created nanogaps in the CNTs through electrical breakdown in air or under Ar flow.^{1,7} This simple approach yields a wide range of nanogaps (from ~ 20 -300 nm) in more than 100 devices. Then, a ~ 10 -nm GST film was sputtered to cover the device surface and fill in the CNT nanogaps,¹ creating lateral PCM bits.

Devices are initially in the OFF state because the as-deposited GST films are amorphous (a-GST) and highly resistive, $R_{\text{OFF}} \sim 50 \text{ M}\Omega$. Voltage applied at the CNT contacts creates a sizeable electric field (E -field) across the nanogap, and switches the GST bit to the crystalline phase (c-GST), which lowers the resistance by about two orders of magnitude, to $R_{\text{ON}} \sim 0.5 \text{ M}\Omega$. Although a-GST covers the entire device, the switching occurs only in the nanogap, which is the location of highest E -field and Joule heating.

To test initial memory switching, we sourced current and measured voltage across the devices (Fig. 1B). The amorphous bits displayed switching at a threshold voltage V_T as is typical with GST,³ and a sharp transformation to a conductive phase



under high E -field. We note that little voltage is dropped across the CNT electrodes, which are much more conductive (~ 50 k Ω) than the GST bit (~ 0.5 - 50 M Ω , depending on phase), as confirmed with detailed finite-element (FE) simulations.^{1,5} Once threshold switching occurs, the bit crystallizes from Joule heating and this marks the SET transition. The SET current was of the order ~ 1 μ A in more than 100 devices tested, which is nearly two orders of magnitude lower than SET currents in conventional PCM.

We examined reversible switching of our devices with pulsed measurements. In Fig. 1C, we plot the resistance after a series of pulses with the same duration (150 ns) and increasing amplitude, starting from the resistive OFF state. The resistance decreases abruptly when the current exceeds

~ 1 μ A, marking the SET transition. The resistance increases again when the current exceeds ~ 5 μ A, which is referred to as the RESET transition. This behavior is consistent with fast melting and quenching of the bit, returning the material to the a-GST phase. Repeated cell switching exhibited good stability after several hundred cycles in devices encapsulated by SiO₂. The lateral CNT-PCM is relatively easy to fabricate, allowing us to study the scaling behavior of more than 100 such devices (Fig. 1D).¹

However, as we sputter a-GST to cover up the entire device, the performance of the CNT-PCM device is inherently limited by the parasitic leakage path between the metal contacts. In order to overcome this problem, we have developed a new method to build CNT-PCM nanowires to eliminate the leakage pathways. This lithography-free technique allows us to fabricate PCM nanowires down to 50 nm width with self-aligned CNT electrodes, as shown in Fig. 2. Two prominent improvements compared to the previous lateral CNT-PCM device are much higher on/off ratio (~ 1000) and more than 5x reduction in SET programming current (~ 0.3 μ A). The latter can be attributed to the much higher OFF-state resistance after eliminating the leakage pathways. Pulse measurements indicate RESET currents of ~ 4 μ A.

3. CONCLUSION

We created lateral CNT-PCM devices and have found that CNTs are excellent PCM electrodes, precisely delivering the programming pulses to nanoscale volumes of GST with very low loss. These lateral devices switch at ~ 1 μ A and ~ 3 V across 20-nm nanogaps, with few μ W programming power (compared to nearly 1 mW in state-of-the-art PCM), enabled by the extremely small volume of GST addressed with a single CNT. Such devices also appear to be very scalable, towards sub- μ A and sub-Volt operation.

In addition, we report a novel technique to fabricate PCM nanowires that are self-aligned with CNT electrodes, which eliminates parasitic current leakage paths and improves device performances with a ~ 5 x reduction in programming current and a ~ 10 x increase in on/off ratio. These two- to three-order of magnitude reduction in power consumptions are extremely encouraging for ultra-low power electronics and memory based on programmable PCM with nanoscale carbon interconnects.

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Biography: Eric Pop is an assistant professor of Electrical and Computer Engineering (ECE) at the University of Illinois Urbana-Champaign (UIUC). His research interests are in low-power nanoelectronics and nanoscale energy transport and conversion. He received his Ph.D. in EE from Stanford (2005), the M.Eng./B.S. in EE and B.S. in Physics from MIT. Between 2005-2007 he did post-doctoral work at Stanford and worked at Intel on non-volatile memory. He received the Presidential Early Career (PECASE) Award from the White House (2010) and Young Investigator Awards from the ONR (2010), NSF (2010), AFOSR (2010) and DARPA (2008). He is an IEEE Senior member and serves on the IEDM and DRC conference program committees.

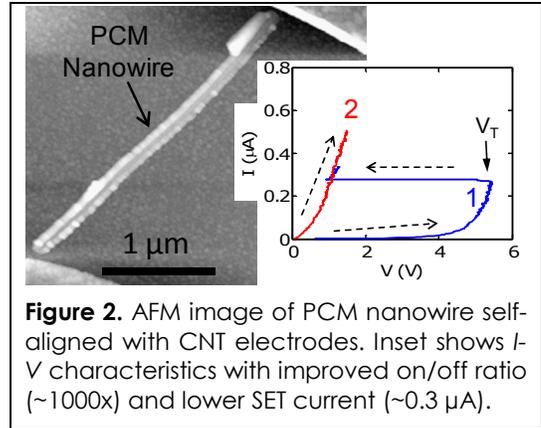


Figure 2. AFM image of PCM nanowire self-aligned with CNT electrodes. Inset shows I - V characteristics with improved on/off ratio (~ 1000 x) and lower SET current (~ 0.3 μ A).