Programming Speed in Ovonic Unified Memory.

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ABSTRACT

Ovonic Unified Memory (OUM) is based on materials in which the phase change (PC) occurs by the application of an electrical signal. In principle OUM devices should be able to replace all electrical memories including those with very strict limitation to the time of programming. Chalcogenide materials used in OUM devices present no fundamental limitations with respect to speed (sub nanoseconds) and to scaling (down to 50 Angstroms) and approaches have been reported to reduce programming currents to acceptable range without sacrificing the memory endurance cycle-life. The aim of this investigation is to find factors affecting programming time and involves studies of the influence of: programming current levels, phase change alloy composition and its thickness, electrode contact materials, device geometry, and temperature. Specific methods of characterizing programming speed will be described for both programming to the set (crystallization or ordering) and reset (amorphization or vitrification) states. It will be shown that programming speed to set or to reset a device is determined mainly by only one of electrical contacts: set speed is not as affected by the cathode contact but depends more strongly on the anode contact and that the reset speed could be changed dramatically with cathode contact (material and geometry) but is not as sensitive to the anode contact.

Key words: phase-change, set-reset speed, crystallizing-amorphizing

1. INTRODUCTION

Phase change technology, which was invented and continuously upgraded by Stan Ovshinsky, is rapidly entering the commercialization phase for non-volatile electric memory [1,2]. Efforts by many groups have accelerated this process [3-8]. It is conductivity and not reflectivity that is of the main importance in phase change alloy composition choice for OUM. Thus the alloy spectrum for OUM is much wider than for optical PC devices [9].
OUM PC technology is based on phase transformations in semiconductor media with bulk negative differential conductivity of S-type (S-NDC) where high-current density filaments appear and switching the material to a highly conducting state is observed [10]. It is a commonly accepted point of view that the filament in OUM device is well formed and that its dynamic resistance is close to 0. Thus any deviations from zero measured on a device's IV (dV/dI at the programming currents range) are due to the total sum of all resistors in series between the probes, including contact resistance

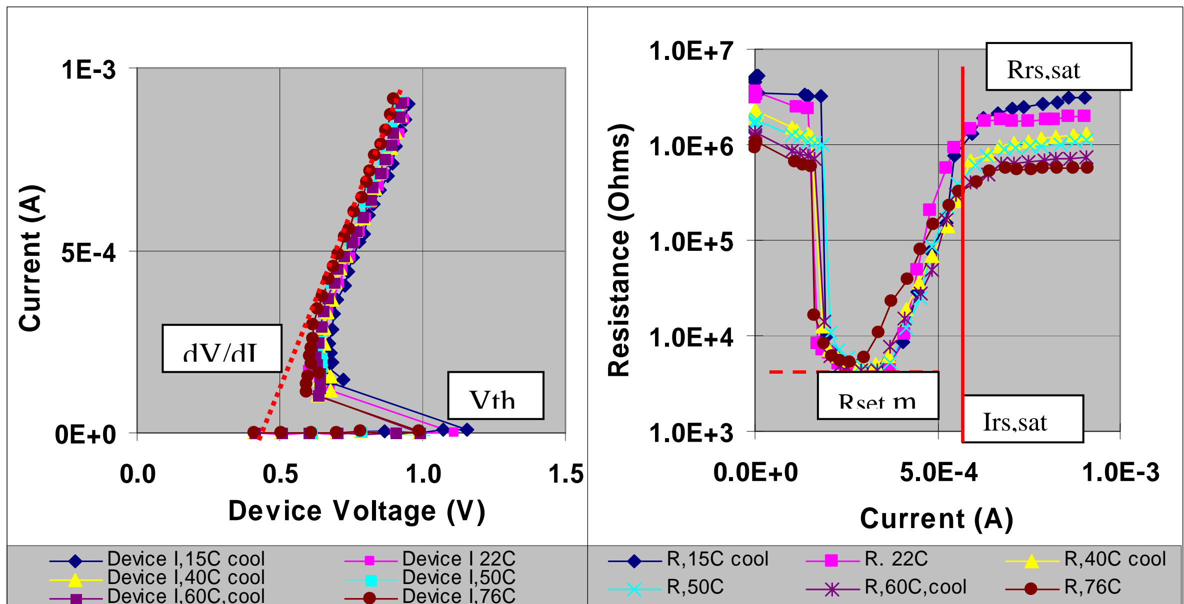


Fig.1 RIVs of typical OUM device for a break-down layer (BDL) device with 225 alloy and Carbon contacts.

With known contact material resistivity and device geometry, dV/dI often coincides with calculated values of the contact resistance and its value doesn't depend on chalcogenide (GST) thickness and temperature. Some variations that do occur can be lumped into an interface resistivity change.

Fig.1 shows typical resistance-current and current-voltage characteristics (RIVs) of an OUM device at different temperatures. These devices are of the "break-down type" which we described previously [11]. We use the data presented for introductory purposes and to establish some definitions. The current value corresponding to the reset resistance (Rrs) saturation (red line) is Irs,sat, and the value of resistance at the RI curve minima (dashed line) shows the set resistance (Rset) which is a low electrical field measurement of the sum all of the resistors between the probes: Rset and the contact resistance, dV/dI. We define Rchalc,min as Rset,min - dV/dI, where dV/dI is measured from the slope of the I-V curve from about 50 to 100% of the reset current (due to possible non-linearity).

In optical memory the programming energy is delivered directly to the phase change media through its surface by a laser beam. In electrical memory devices it is delivered by an electrical signal through metallic or semi-metallic contacts [12,13,15]. S-NDC enhances the role of inhomogeneities [15,16]. The rest of this paper describes the relationship between these parameters and programming speed.

2. EXPERIMENTS

Four different type devices were used in the following experiments. The structure of the legacy ECD breakdown type and the offset pore type were reported previously [4]. In addition, we also report on data from more recent Ovonyx processed devices made by e-beam lithography and with break-down layers.

Measurement Method for RESET SPEED

We typically measure reset speed by applying optimized SET pulses and vary the width of optimized RESET pulses as shown in Figure 2a. The optimized amplitudes are obtained from RIVs measured on similar devices. The data are collected by varying the reset pulse width (10ns - 500ns) with its amplitude as a parameter. The low field device resistance is measured with a small DC bias after each pulse. Finally, RESET SPEED is defined as a ratio of Ireset at which Rrst on Rrst vs. Wreset falls below 20ns to Irs,sat from Fig.2b. In other words, we define reset speed as the ratio of Irs at which Rrs vs. Wrs crosses the demarcation line Wrs=20ns to Irs,sat (Fig.1). The lower this number, the faster is the reset speed.

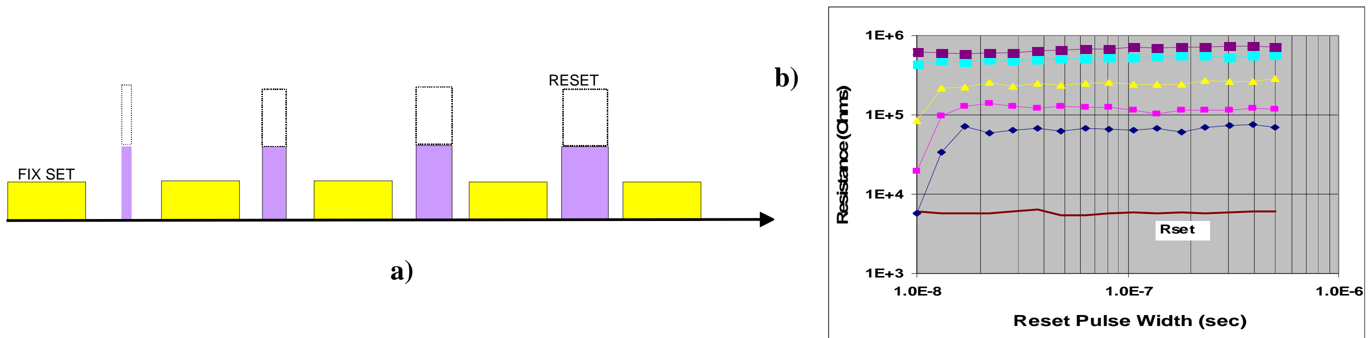
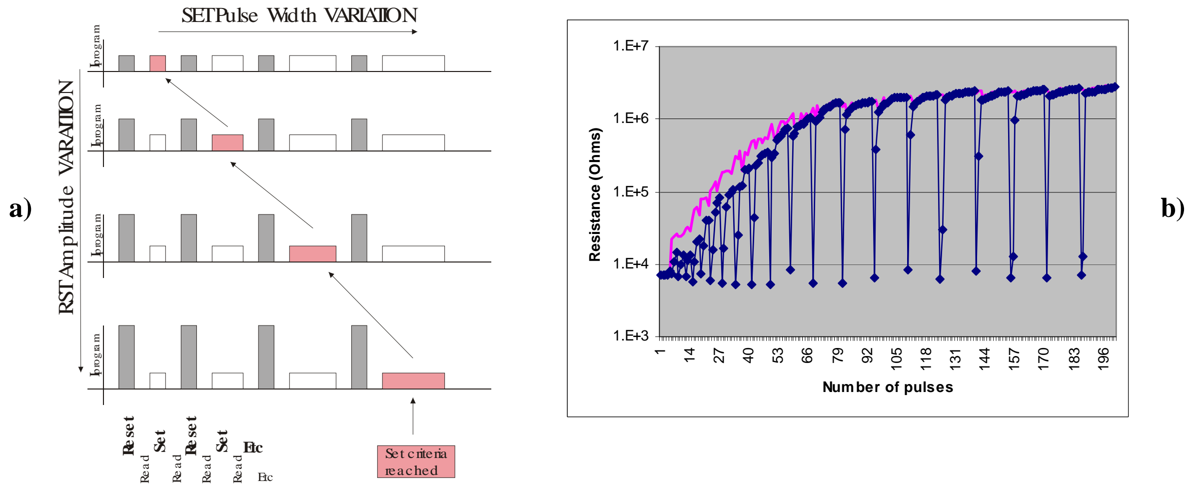


Fig.2 a) Reset speed test scheme. Fixed are: set pulse (width and amplitude) and reset pulse amplitude, b) Example of Rrst vs. reset pulse width with different reset amplitude.

Universal Measurement Method for SET SPEED

We describe the SET SPEED method schematically in Figure 3a. A fixed reset amplitude and pulse width is applied with a fixed amplitude and increasing SET PULSE width. Since the device starts out SET, the target value for a set resistance, Rset,target, is reached almost immediately. Next the RESET amplitude is increased (RESET pulse width remains fixed through out the test) and it takes wider and wider set pulses to SET the device because it is being reset more and more. The target SET resistance is determined as: Rset,target = 10^ {log(Rset) + [log(Rrs/Rset)]/6 }. The SET-PW required to set below the Rset-target is plotted vs. Irs together with the RI curve and is shown in Figure 5b.Saturated values of Rrst are determined from the device RIVs, and thus Irst,sat and Irs,sat + 20% "over-reset" are determined.

Fig.3 Set speed test scheme (a) and example of raw data (b)



3. RESULTS and DISCUSSION

We now present results of an experimental study of phase change kinetics from amorphous to crystalline transitions for various GeSbTe film thicknesses, ranging from 13 to 100 nm. First we show that the reset resistance of a pore device can be calculated from the geometry presented by an up side down cone with truncated top. Its resistance is given by:
$R = (\rho * d)/(\pi * r(r+d/tg\alpha))$, where r is the radius of bottom contact, d is the GST thickness and α is related to spreading and is taken to be 45°.
Fig.4 a, shows experimental data and the scaling of Rreset,sat with GST thickness. As can be seen, Rrst,sat fits the above expression with a pore diameter of 2r = 2000 Angstrom. Scaling of the threshold voltage of switching of reset devices with GST thickness [14] also verified that the whole thickness of the device was involved in the phase transition. On the other hand, set resistance after subtraction of dV/dI doesn't scale with thickness of GST. This suggests the presence of higher low-field resistivity layer independent on GST thickness.

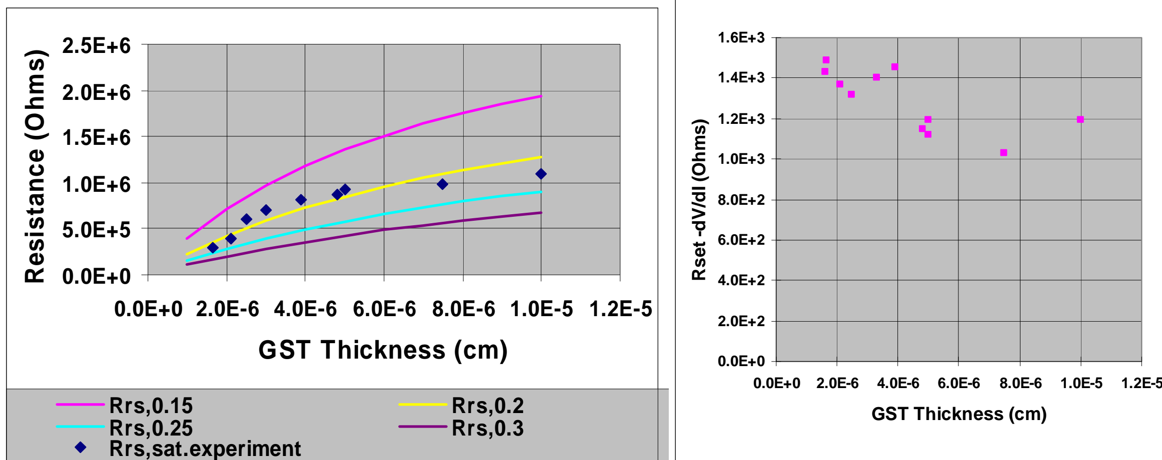


Fig.4 Calculated and experimental Rrs,sat and Rset – dV/dI vs. GST thickness

We now turn to the "time to crystallize," as defined by the set pulse width needed to set the device to a target level from a given starting RESET resistance, which is shown in Fig.5. Starting with a nearly SET device the required set pulse width rises almost exponentially: Wset = Wset,min.exp(GRrs), (where G is characteristic conductance) with some intermediate saturation and finally vertically at seemingly the same Rrs. The rise in SET pulse width is seen when the remaining volume fraction of crystallites in the device decreases. We believe the vertical rise in pulse width appears at reset resistance corresponding to the loss of nuclei, e.g. no remaining crystallites.

Previously we reported [14] that Wset,min scales with chalcogenide thickness and this allowed us to suggest that crystallization front propagates through the bulk of GST between contacts along the current path with approximate speed of 600cm/sec. So on one hand Rchalc,min doesn't scale with GST thickness and on the other hand crystalline material seems to propagate from one contact to another. These two observations taken together suggest that the region mostly responsible for Rset is located at one of contacts. We believe the dominant component of Rset is located at the top electrode interface and crystalline material serves as a virtual contact to it. The effective area of the virtual contact to this interface will depend on low-field resistance of interface and Rset,target. Higher interface resistance larger is the volume fraction of crystalline material. Lower Rset,target also demands higher volume fraction of crystalline material. These volume fractions will be

a) b)

Fig.5 Set pulse width dependence on reset resistance (a) and on programming current (b). BDL device with C-C contacts

higher than in a case with no resistive interface present. Thus the presence of a resistive interface reduces shunting effect of crystalline "needles" on the amorphous dome.

Contact material, device geometry, and alloy effects. Figures 6a and 6b and Figures 7a nd 7b show reset and set resistance vs. corresponding pulse width and amplitude for two different types of devices made with the same chalcogenide alloy but with different geometries and different contact materials. The inserts show the devices schematically with materials and geometry of contacts.

Comparing these two figures we note the dramatic difference in the RESET characteristics between the two device types. In the BDL devices Rrst shows no dependence on reset pulse width and varies ONLY with the reset pulse amplitude. In another words BDL device demonstrates that in the range of pulse width 30ns – 10ms only the pulse power programs the device into a reset state and defines the Rrst value.

a) b)

Figure 6 a) Reset resistance vs. Pulse width for different reset current for a break-down device with C-C contacts, and b) Set resistance vs. set pulse width and amplitude (Iset) at fixed reset

In the lateral offset device the RESET data is completely different. Here, a certain pulse width time for a full Rrst level is easily seen and depends on the amplitude of the pulse AND the pulse width.
With high enough programming current, RESET speed on both type of devices is similar.
Set behavior of these two groups is also distinct and is very similar if set current was chosen to be on the left-hand side of RI Ith<Iset<Imin, where Ith is threshold current of switching, Imin is a current corresponding to a minima of RI.

a) **b)**

Fig. 7 a) Reset resistance vs. Pulse width with different reset current for a lateral device with TiAlN bottom and TiW top contacts, and b) Set resistance vs. set pulse width and amplitude (Iset) at fixed reset.

What can modify the set speed of OUM device? It is natural to assume that if we provide a low resistance (ohmic) contact electrode interface, that Rset, Vh, and Wset will be reduced. There are several alternatives; change the alloy composition with the same contact materials, change the contact material, introduce an ohmic intermediate low R contacting layer between the GST and electrical contact, or a combination of these.
Table 1 presents some experimental data.

ALLOY	Bottom Electrical Contact (BEC)	Top Electrical Contact (TEC)	Wset at Irs,sat (sec)	Wset at 1.2Isat (sec)	Reset speed: Irs,min 20ns /Irs,sat,
225 old BDL	C	C	3e-7	3e-6	0.4
225 old lateral	TiAlN 2mΩ cm	TiW	3e-7	2.8e-6	2.7
225 FF BDL	TiAlN 5mΩ cm	Ti-TiN-Ti	3e-8	7e-8	1.2
LRA* FF BDL	TiAlN 5mΩ cm	Ti-TiN-Ti	1.5e-8	4e-8	1.35
LRA FF BDL	TiAlN-C	Ti-TiN-Ti	2e-8	4e-8	1.1
LRA E-beam	C	C-MoN	4e-8	5e-8	1.2
LRA E-beam	MoN	C-MoN	5e-8	2e-7	1.5

* LRA – Low Resistivity phase change Alloy

From the above data we can make the following conclusions. Changing to a lower resistance alloy improves set speed especially at 1.2Irs,sat. The bottom contact material and resistance has less influence on Set-speed. Addition of a Ti layer to the top contact greatly improves set speed. This is likely related to Ti incorporation into the 225 film coupled with providing a good ohmic upper contact (weak interface). Reset speed is little affected by top contact modifications but depends on the conductivity of the bottom contact and the memory alloy. Conductivity of LRA is higher and reset speed is faster even with C-C contacts.

Polarity. With very weak or no interface resistance, a small crystalline filament would be enough to shunt the device and Rset should scale with GST thickness. The positive contact interface area could be changed in asymmetrical devices by changing polarity of programming and read voltage by swapping probes. Indeed numerous examples on C-C BDL devices and direct contact devices show that changing the polarity almost immediately (after the first reset event) brings a significant change in Rset value. We believe this is due to an effective change of interface area (due to device asymmetry).

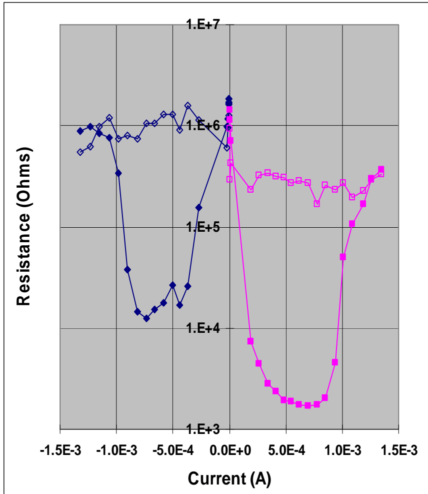


Fig.8. Positive and negative polarity RIs of wired BDL device with C-C contacts

Temperature dependence of programming speed

The reset resistance varies with temperature because carrier generation in the GST is an activated process. Therefore, when we look at Figure 9a we see different starting reset levels. As the pulse width to SET is increased at each temperature, each of the curves drops down to the SET level. The SET speed, defined as the pulse width needed to reach a certain resistance level, decreases with temperature – the device becomes faster.

a) **b)**

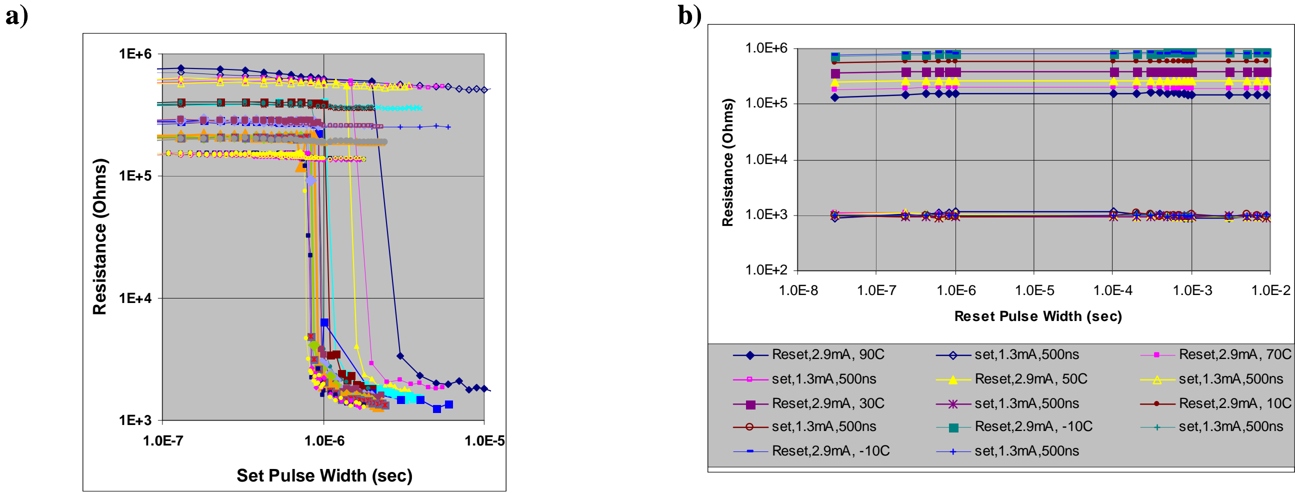


Fig. 9 a) SET speed vs temperature and b) RESET pulse width dependence in a temperature range 10 – 90°C for a BDL device with C-C contacts and incorporating 225 alloy.

Rset - dV/dI, Iset, and Irs are practically independent on temperature. Increasing of programmed resistance is accompanied with a continuous rise in activation energy;

Set pulse width decreases with increasing T with activation energy ranging from 0.05 to 0.3 eV (Fig. 9a)

For C-C contact devices Reset pulse width is independent on T in a range 20nsec – 10msec (Fig. 9b)

Forming of C-C contacts

For completeness, we add data to show that carbon contacts are quite unique as electrode materials. The uniqueness is based on FORMING, or the change of CARBON from a relatively resistive material to a highly conducting one, but only in

the vicinity of the contact region. Joule heating by passing current through a C-SiNx-C stack causes the change. The SiNx acts as a break-down layer which localizes the device operation to the vicinity of the break-down. Figure 10 shows that as current passes through the device, it becomes more and more conductive and that the change is permanent. Staring at 1e6 ohms, a breakdown occurs at 2mA (about 3v) and the device changes to 1e4 ohms. Further increase in current cause the devices to drop to 1e3 and finally to 100 ohms. Annealing these devices at 350C for 72hrs (Table 2) results in no further changes. Also annealing virgin devices at low temperatures of 350C does not cause them to be as conductive. We thus conclude that we have FORMED the carbon in the vicinity of the break-down region where programming temperatures reach 650-700C. This provides the benefit of isotropic heat conduction, much higher normal to the surface than lateral, helping to effectively thermally isolate the device. This experiment suggests that Carbon contacts ONLY change resistance along the current path and stay more resistive both electrically and thermally away from the current path. Thus lateral heat losses through contact thickness are minimized and we believe this is what makes the difference between C-C BDL devices and TiAlN bottom contact lateral devices. Note that reset speed improves (faster) if bottom contact uses TiAlN with higher resistivity.

Fig. 10 Electrical forming of C-SiNx-C cell

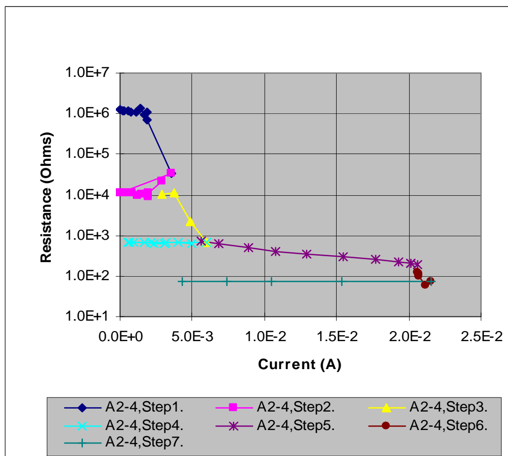


Table 2.

Virgin resistance. Wafer A2 (C-SiNx-C)	Resistance after an application of electrical pulses	Resistance of the same devices after annealing at 350 C for 72 hours (slow cooling)
1.96e6.	444	511
1.25e6	3.46e4	3.42e4
8.15e5	1.5e4	1.4e4
1.56e6	210	289
2.7e6	814	886
1.7e6	Left virgin	1.3e5
1.2e6	Left virgin	9.1e4
1.4e6	Left virgin	9.4e4
9,6e5	Left virgin	8.5e4

4. Conclusions

Rrst scales with GST thickness but Rset minus dV/dI doesn't. Rset-dV/dI is interface resistance at low field. The PC alloy crystalline regions are ONLY a virtual contact to the top electrode interface. Wset is not just a crystallization time but also a time for the crystalline region to reach a certain volume and make wider contact to the electrode interface to meet Rset,target criteria. This interface is located at the top contact of the device and when we make it weaker (less resistive) with top contact or alloy material we increase the set speed. Polarity experiments also show the location of interface resistance. Reset speed is defined mostly by lateral heat losses through the bottom contact and adjacent GST as shown by experiments with lateral conductive contact device and with lower resistivity material. OUM devices could be programmed with higher set speed if the interface resistance is reduced (less resistive) either by choosing "Ohmic" top contact or using lower resistivity memory alloy. Both should sustain multiple thermal cycling without oxidation or morphology changes. Higher reset speed of OUM devices is possible when lateral heat losses of a bottom contact and a chalcogenide material adjacent to bottom contact are minimized. A very useful property of amorphous carbon is its ability to undergo an unidirectional change of resistivity only along the current path. This makes Carbon desirable for bottom electrode contacts. Top electrode contact material should be chosen based on the conductivity of a memory alloy adjacent to it to minimize low-field interface resistance.

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Biographies

Wally Czubatyj, Director of Engineering – Ovonyx Technologies, Inc.

Wally Czubatyj was born in Germany in 1946. He got his PhD in Electrical Engineering from Wayne State University in 1977 and started his professional career at Energy Conversion Devices. As a research scientist, he pursued his interests in thin films, photovoltaics and chalcogenides with emphasis on microelectronic devices. After several years as a research scientist he became the program manager and then the director of the microelectronics group, where he was able to pursue novel device development. In the mid to late 80s, his interests changed from amorphous silicon for solar cell and display applications to chalcogenides for microelectronic applications in the switching and memory areas. His 1989 proposal to investigate devices based on new congruent crystallizing chalcogenide materials for radiation hard non-volatile memory applications renewed interest in the electronic chalcogenide memory program where he has worked ever since. During the 1990's he led the effort at ECD to reduce the programming current in chalcogenide based memory devices and in 1999 he joined Ovonyx Inc. to pursue commercialization of these devices. At OTI he continues to research memory devices and materials as well as work toward development and commercialization of non-volatile memory products. He currently has 22 issued patents, 7 applied for and others pending.

Tyler Lowrey, President, Chief Executive Officer and Director – Ovonyx, Inc.

Mr. Lowrey has overall responsibility for the Company and its projects, alliances, outside investors, investments and day-to-day operations. The Company is chartered with commercializing chalcogenide phase-change nonvolatile memory devices that the Company calls Ovonic Unified Memory ("OUM"). He is the inventor/co-inventor of more than 100 U.S. patents related to semiconductor memories and more than 30 OUM-related patent disclosures. Mr. Lowrey has an extensive background in solid-state IC memories and their development, debug and ramp-up to high-volume competitive production. He served as a process engineer and device engineer and in mid-level and senior-level management positions at Micron Technology, a Fortune 500 memory producer. While at Micron, he was Vice President-Chief Technical Officer and Vice President-Chief Operating Officer as well as a director and Vice Chairman of Micron's board of directors. As part of the Company's joint development programs with the Company's licensees, Mr. Lowrey assists to evaluate, debug and optimize the processes, materials, devices and cell structures – with particular attention to processes and electrical characterizations. Mr. Lowrey is presently on the Board of Directors of Litel Corp.

Sergey Kostylev was born in Dnepropetrovsk, Ukraine. Received B.S. and M.S. in physics and mathematics and Ph.D. in physics of semiconductors and insulators (PSI) from Dnepropetrovsk state university, Ukraine in 1959 and 1966 respectively and Doctor of Science in PSI from Moscow Institute of Radio-electronics and Engineering of Academy of Sciences of USSR and the Highest Qualifying Commission of USSR in 1982.

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