

Recent Advances in Conduction Mode Scanning Probes for Phase Change Probe Storage Applications

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ABSTRACT

In this paper, recent progress in improving conduction mode scanning probe technology is summarized. In particular, the development of platinum silicide nanoscale tips, their encapsulation in a dielectric, and the associated improvement in tip current density and reliability are described. Modeling results of nanoscale contact resistance and of the phase change phenomenon using such probes are also presented. Finally, results on the long term conduction reliability of these probes are reviewed, and their use in phase change probe storage and materials characterization is discussed.

Key words: Conducting Cantilever Probes, Phase Change, Probe Storage, Materials Characterization

1. INTRODUCTION

Data storage that employs cantilever probes to read and write data on a medium has been proposed previously and significant progress has been made in recent years to realize devices based on this concept^{1,6}. According to this concept, several of these probes operate in parallel and locally modify the surface and/or the material properties of a suitable medium. These modifications are then used as information carriers for data storage applications. In this paper, we focus on probe storage that uses phase change media³⁻⁵. This technology, also occasionally termed electrical probe storage⁵, is promising for all the same reasons that phase change memory has been of great interest— speed, density and cost. In electrical probe storage, an atomic force microscope (AFM) probe with a conducting tip is used to modify the phase in a localized region of a phase change film. The phase change material used is most commonly a GeSbTe-based alloy of the form Ge₂Sb₂Te₅, henceforth referred to as GST. In electrical probe storage, the GST layer is often protected by a capping layer to prevent its oxidation.

While probe-based storage technology for mobile applications using polymer media has reached a certain level of maturity⁶, it has a rather small cost advantage when compared to flash memory, the dominant incumbent non-volatile memory technology. Hence, it would have been challenging to enter the very competitive mobile storage with a radically new technology. On the other hand, the archival storage market is dominated by tape drives. The areal and/or volumetric density of tape drives, and hence the cartridge capacity, while increasing steadily, might not be adequate to meet the explosive growth of archival data. The volumetric density improvement in tape drives is expected to be approximately 40% per year for the next 10 years. This potentially presents an opportunity for a disruptive technology that can offer ultra-high aerial or volumetric densities. Thus, if the cost of the micromechanical components in probe storage could be amortized over a larger recording area, probe storage would be able to provide much higher device capacity at a much lower cost/ GB (see Figure 1). This would be a very attractive value proposition, as the sheer volume of archival data is expected to be overwhelming in just a few years.

The polymer-based thermomechanical writing and reading process¹ is limited by the microsecond-scale thermomechanical time constant of the heater probe, which limits the data rate per probe. This limit necessitates much higher parallelism, which could potentially result in greater system complexity. By using phase change media, which

can be switched in a few nanoseconds, the amount of parallelism required can be greatly reduced. Moreover, multi-level recording using probes may be possible, which would increase density and thus storage capacity. Further, it is very difficult to erase a bit written on an amorphous background of the phase change material. This could be an enabling factor for many archival applications that require true, write-once-read-many (WORM) functionality. At the same time, the phase change probe recording has a very serious drawback – the reliability of the probe-tips, which must maintain nanoscale structural integrity while still being able to deliver current reliably to the underlying phase change material. Significant steps towards addressing this issue are reported in this paper.

Phase change materials, particularly GST, are already of interest for future memory devices⁷. Therefore, in addition to electrical probe storage, a by-product of the use of probes on phase change media is the understanding of the physics of sub-threshold conduction and the phenomenon of threshold switching. In addition, various types of phase change media, and electrode materials can be studied and characterized rapidly. This could be useful in designing future memory devices.

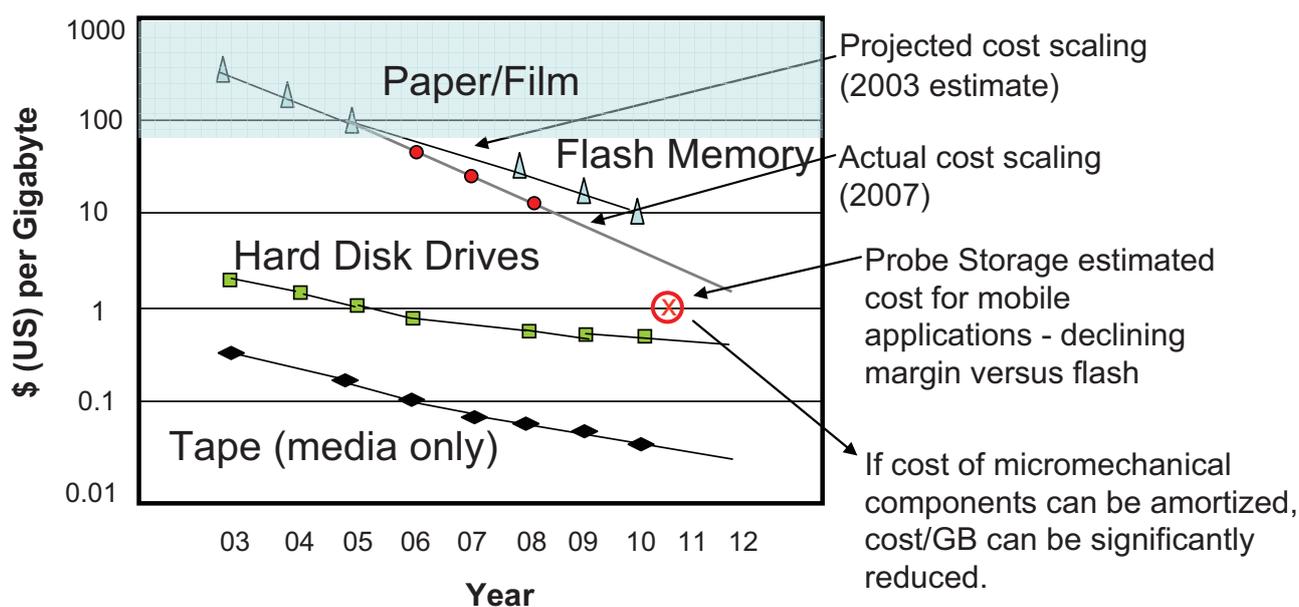


Figure 1 Cost/ GB of different types of storage and the year of availability.

2. NANOSCALE TIP ENGINEERING

Previous reports have shown how the reliability of conducting probes can be improved by carefully engineering the tip. This has been accomplished by the use of platinum silicide (PtSi) tip apexes, which were shown to be superior to commercial Pt-Ir tips in terms of both wear, as well as conduction properties⁸. In addition, these nanoscale tips show a current carrying capacity far greater than that of tips of comparable diameter (~1 mA for tips of ~25 nm radius). An additional advantage of these tips is the ability to manufacture them in standard bulk processing facilities, without use of nanoscale patterning or advanced lithography techniques. An image of such a tip with a PtSi apex is shown in Figure 2a.

Because studies on films of phase change materials using conducting probes are typically carried out on flat surfaces, the physical ability of a tip to probe nanoscale asperities is not an added functionality. However, the nanoscale dimension of the conductor enables one to observe nanoscale phase transformations using an electrical pulse. Thus a tip that has a large physical diameter, but a much smaller conducting region would be ideal for wear reduction as well as nanoscale conduction. This is simply because of the reduced pressure at the tip that contributes to lower levels of wear. In Figure 2b, we show a PtSi tip after being used for several thousands of read-write cycles. The wear on such a tip is observed to be quite large and certainly not commensurate with the requirements for probe storage. In order to overcome this severe wear issue, the concept of an encapsulated tip was introduced, and one such tip is shown in

Figure 2c. Such tips exhibit stable conduction for 2.5 m of sliding⁹. In addition, the wear on the encapsulated region of such a tip is shown to be negligible for 10 m. This is a phenomenal improvement in wear resistance over commercially available conducting tips, but much greater sliding distance performance evaluations are necessary to verify that their reliability would meet the demands of archival probe storage. The fabrication and the details of the reliability evaluation of these tips are described in [9].

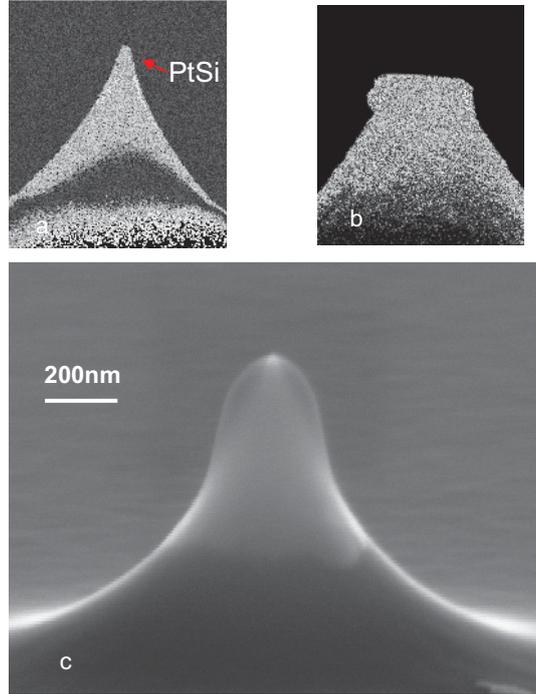


Figure 2 a. PtSi tip; b. Worn PtSi tip and c. PtSi tip encapsulated in SiO₂.

To demonstrate the superiority of PtSi tips to regular Si tips in terms of contact resistance, we perform current-voltage (I-V) measurements on Au, and such a comparison, as reported in [8], is shown in Figure 3. To verify the experimental values, modeling of the contact resistance was carried out. The total resistance can be modelled as being made up of tip resistance, contact resistance, and the sample resistance (Au in this case). The tip resistance can be mathematically calculated through integration, whereas the sample resistance can be calculated using $R_{sample} = \rho_{Au}/2d$, where ρ_{Au} and d are the resistivity and the thickness of the sample, respectively. The contact resistance between the tip and sample can be estimated by $R_{contact} = (\rho_{Au} + \rho_{tip})/(4a_{contact})$, where ρ_{tip} is the resistivity of the tip, and $a_{contact}$ is the contact radius¹⁰. $a_{contact}$ is calculated using the following expression¹¹:

$$a_{contact} = \left(r^2 - \left(r - \left(\frac{9F^2}{16rE^*} \right)^{1/3} \right)^2 \right)^{1/2} \quad (1)$$

Where r is the radius of a smooth sphere at the bottom of the tip, F is the tip loading force, and E^* is the equivalent Young's modulus of elasticity. Using these simplified calculations we evaluate the contact resistance, and consequently the I-V characteristic on Au, and find that it agrees well to the measured values, as shown in Figure 3.

3. PROBE-BASED PHASE TRANSFORMATIONS

Because the phase transformation in phase change materials occurs due to the Joule heating of the GST, it is important that this heating be localized in order to confine the size of the bit. The use of encapsulated probes, as opposed to standard PtSi probes, presents an additional challenge as the heat can also propagate transversely in the encapsulating oxide, near the interface of the tip and the storage medium. This could result in the enlargement of the bit, even though the thermal conductivity of the encapsulating SiO₂ is very poor. In order to verify that the effect of the

encapsulation on bit size is not a major one, we performed modeling of the bit shape using both PtSi as well as encapsulated tips. A simple empirical model, as described by Wright et al.⁴ and a more involved analytical model as described by Ielmini et al.¹² were used to study the effect of encapsulation on bit shape. The writing was simulated on a stack with the configuration shown in Figure 4a. The radius of the tip for the simulation was assumed to be 20 nm. The analytical model predicts a bit that would be approximately 20% larger in diameter when using an encapsulated bit. The results of the modeling are shown in Figures 4b (using the empirical model by Wright et al) and 4c (using the analytical model by Ielmini et al).

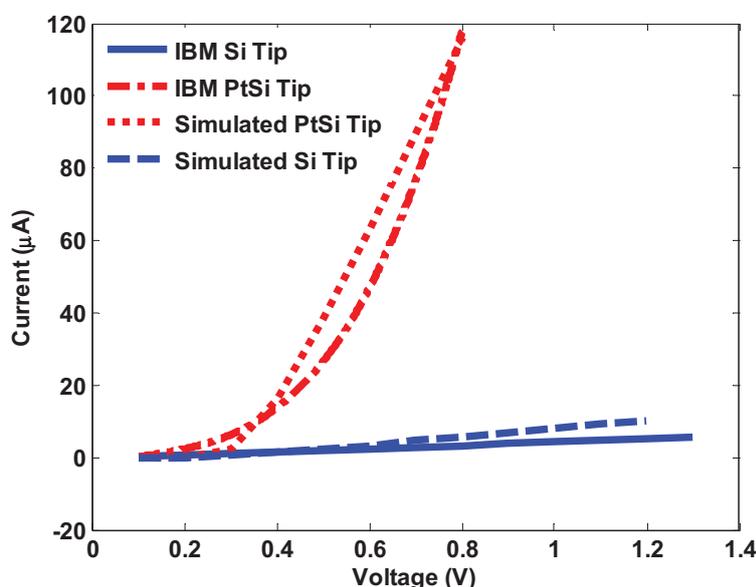


Figure 3 Contact Resistance of the tip on Au. The model agrees well with the experiment.

We then perform bit writing experiments on stacks of amorphous $\text{Ge}_2\text{Sb}_2\text{Te}_5$ with a bottom electrode and a capping layer. The stack configuration is the same as that shown in Figure 4a. The top and bottom electrodes are both sputtered carbon, the conductivity of which has been increased by introducing nitrogen gas during the sputtering process. All layers were sputtered in vacuum connected chambers, so as to prevent any degradation due to oxidation of the GST. Bit writing is accomplished using a home-built atomic force microscope. The cantilever and the sample are both electrically connected to an external electronics board that has data acquisition cards as well as to a pulse generator. A logarithmic amplifier is also part of the electronics board and allows one to dynamically measure resistances of both the amorphous, as well as the crystalline regions whilst scanning. A single bit is written by applying a voltage greater than the threshold voltage, which was determined to be around 3V for this particular stack. Bits are crystalline regions of lower resistivity as compared to the amorphous, highly resistive background material that we start with. Reading is accomplished by scanning at a voltage lower than the threshold voltage (500mV).

In order to verify that the bit sizes are affected mostly by the conducting core and not by the encapsulation, we start with a tip that has a small protrusion through the encapsulation, as shown in Figure 5 (left tip image within the graph). The tip is then worn by continuously writing and reading bits on the surface. The wear is monitored by monitoring the force of adhesion after a sequence of writes and reads. The force of adhesion, being proportional to the physical diameter of the tip, would indicate when the encapsulation is reached. After the last write-read sequence, we remove the cantilever and image the tip once again. This helps verify that the final bits were written while the tips were encapsulated. The graph of evolution of the adhesive force as a function of sliding distance along with a tip before and after the whole range of experiments is shown in Figure 5. As the tip reaches the encapsulation wear slows down. The final image of the tip is shown in the figure. The results of the bit writing experiments using both tips are also shown in the same figure. It is seen that in the deflection images, where the topography is imaged using the deflection signal

of the cantilever, the surface roughness of the carbon is very well resolved with the sharp tip. At the same time, the conduction images of the written bits confirm that we can perform read and write operations using both types of tips.

Once the tip wears, we find that in the deflection image, small topographical features cannot be resolved due to the convolution effect with the encapsulated tips, which has a larger diameter than the protruded tip; however, the conduction images of bits written using this tip still show that the size of the bit corresponds to the diameter of the conducting core. The diameter of the conducting core is less than 10% smaller than the size of the written bit. Thus experimentally, we have observed that the bit sizes are not significantly affected by the encapsulation.

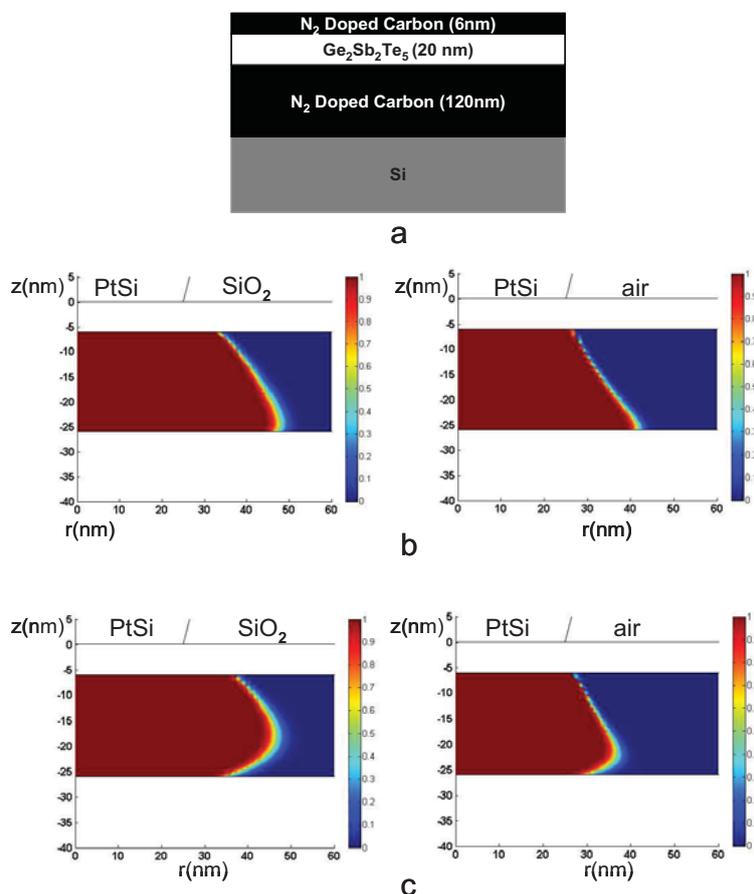


Figure 4 a. Phase Change Stack used for the experiments; b. Simulations of bit sizes using both standard PtSi tips (right) as well as Encapsulated tips (left) using the empirical model (Wright et al³) and c. the analytical model (Ielmini et al¹¹).

Using the modeling approach described in the previous section, we have made efforts towards understanding the threshold voltage behavior of these materials. The results of modeling the I-V characteristic are shown alongside the experimental I-V characteristic in Figure 6. It is seen that the analytical model of Ielmini et al¹¹ is closer to the experimental values, although both models underestimate the value of the threshold voltage. This could be due to a number of reasons, most probably involving the uncertainty in the values of resistivity of the capping and bottom layers of the materials. Underestimating these values in the model could increase the value of the electrical field, thus underestimating the threshold voltage. It is worthwhile mentioning that in these models, we have not incorporated the contact resistance calculations as described in the previous section. Incorporation of those would also improve the analytical model predictions. Nevertheless, it is seen that the analytical model captures the experimental observation of threshold switching. Much more work on understanding and incorporating all of the contributing phenomena is necessary towards unraveling the dynamics of the phase change process.

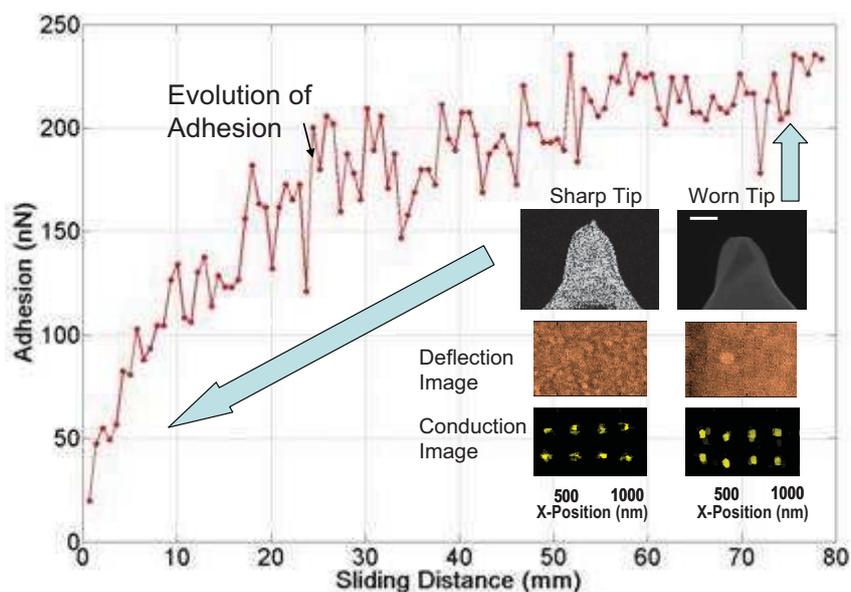


Figure 5 Wear of a tip with a sharp projection of the conducting core. The force of adhesion increases as the tip wears down to the encapsulation. The SEM images of the tip before and after the wear experiment is shown. Below the SEM images of the tips are the corresponding deflection and conduction images of the regions in which the bits were written. We write new bits for every image, thus the two sets of bits are distinct.

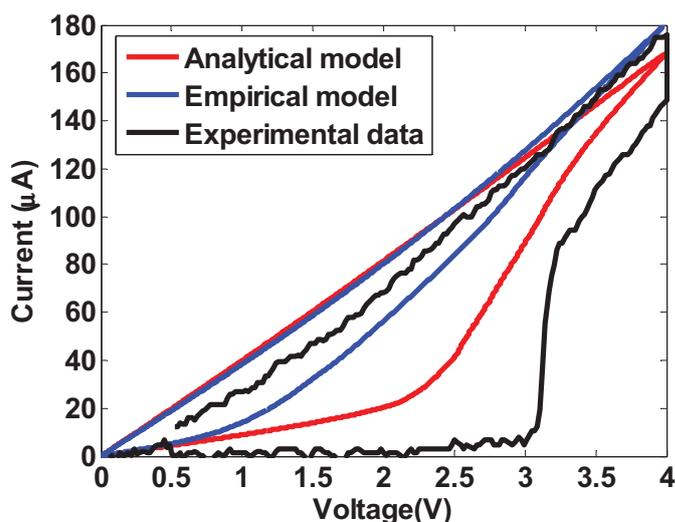


Figure 6 I-V characteristics of the phase change material using conducting probes - experimental, as well as modeled values of threshold voltage are obtained.

Finally, we sought to exploit the large adhesion at the apex of the encapsulated tip, owing to the larger physical diameter, by reading the written data in retraction mode. In this mode, we take advantage of the rather large distance to snap-off due to the high force of adhesion. We then accomplish scanning in this regime, where the cantilever is retracted after being brought into contact. We have accomplished reading bits with a retraction force of 100 nN, on a tip that had a tip-sample adhesion of ~ 200 nN. The methodology and experimental results to read bits in this mode of operation are detailed in [13]. Scanning in retraction mode is especially advantageous for archival storage using large arrays, because once the cantilevers are brought into contact, large variations due to wafer bow or stress on the

medium would not result in the cantilevers snapping off the surface. This could thus become an enabling technology for implementing large probe arrays for archival data storage.

4. CONCLUSION

In conclusion, we present recent progress toward improving the reliability at the nanoscale interface of a conducting tip and the sample by carefully engineering the tip. We show that the concept of encapsulation increases the tip reliability by two orders of magnitude compared to standard tips of nanoscale dimensions available commercially. Using the novel conducting tips, we perform phase transformations in $\text{Ge}_2\text{Sb}_2\text{Te}_5$, a commonly used material in phase change memory and optical storage devices. We use these phase transformation experiments to demonstrate the suitability of these probes for electrical probe storage. In addition, modeling of the phase transformation using probes facilitates the understanding of the mechanisms of sub-threshold conduction and threshold switching. In future, we shall continue to use conducting probe based phase transformation in such films to understand nanoscale behavior of phase change materials, and help refine the models necessary to predict threshold switching. The insights gained from such efforts would help in evaluating the relative merits of probe-based data storage using phase change media in archival storage applications.

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REFERENCES

1. P. Vettiger, G. Cross, M. Despont, et al., *IEEE Trans. Nanotech.*, 1, 39 (2002).
2. E. Eleftheriou, T. Antonakopoulos, G. K. Binnig, et al., "Millipede—A MEMS Based Scanning-Probe Data Storage System," *IEEE Trans. Magn.* vol. 39, no. 2, 938–945 (2003).
3. H. Kado and T. Tohda, *Jpn. J. Appl. Phys.* 36, 1 (1997).
4. C. D. Wright, M. Armand, and M. M. Aziz, "Terabit-per-square-inch data storage using phase-change media and scanning electrical nanopores," *IEEE Trans. Nanotech.*, 5, 1, (2006).
5. S. Gidon, O. Lemonnier, B. Roland, O. Bichet and C. Dressler, *Appl. Phys. Lett.*, 85, 26 (2004).
6. A. Pantazi, A. Sebastian et al, *IBM J. Res. Develop.*, 52, 4/5, Page 493 (2008).
7. S. Raoux, G. W. Burr, et al, *IBM J. Res. Develop.* 52, 4/5, 465 (2008).
8. H. Bhaskaran, A. Sebastian, M. Despont, *IEEE Trans. Nanotech.* 8(1), 131 (2009).
9. H. Bhaskaran, A. Sebastian, U. Drechsler and M. Despont, *Nanotechnology* 20 105701 (2009).
10. B. Bhushan, *Nanotribology and Nanomechanics: An Introduction*, Springer, 2007.
11. H. Lo, and J. A. Bain, "Effects of high current density at nanoscale point contacts," *Proceedings of MNHT2008, Micro/Nanoscale heat transfer international conference*, 2008.
12. Ielmini, D. and Zhang, Y. G., "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *J. Appl. Phys.*, vol. 102, pp. 054517-1-054517-13, 2007.
13. H. Bhaskaran, A. Sebastian, A. Pauza et al, *Rev. Sci. Instrum.* 80, 8 (to appear).

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