Reliability Characterization of Phase Change Memory

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Introduction

Over the past decade, chalcogenide-based non-volatile memory (NVM) development has progressed from studies of single cell behavior to large memory arrays [1]. This memory technology, referred to as Phase Change Memory (PCM), has now reached the point of commercialization. While studies of cell-level reliability have shown PCM to be more than capable of meeting the requirements for a typical NVM (like floating-gate based Flash memory) and to approach the requirements for DRAM, the reliability of large array products is typically determined by the behavior of a few cells that exhibit either extrinsic weakness or are at the end of a broad intrinsic distribution. Understanding and improving the reliability of these cells then becomes the limiting factor to successful deployment of the technology in reliable products. These improvements can be achieved by optimization of the materials and processes to produce the cells as well as the methods use to program the cells. This paper presents the results of reliability characterization on large PCM arrays, discussing the failure mechanisms seen in early-failing cells and how optimization of both the process technology and device operation can produce reliable large array products.

Reliability Considerations

PCM cell reliability risks can be generically grouped into three types: Data retention, cycling endurance, and data disturbs. Data retention refers to the ability of the device to retain the data written into the cell over a prescribed period of time (and typically at a maximum ambient temperature). Cycling endurance is the number of re-writes that can be applied to the cell without failure. And data disturb is the ability to access a cell or neighboring cells without un-intentionally changing the stored data. PCM performs well in each of these areas. It shows data retention capability to 10 years that is independent of cycling (while, for example, floating gate devices show a reduction in retention as they are cycled). Cycling endurance is on the order of 10^8 writes, significantly higher than the ~10^5 specified for floating gate technologies [2]. And finally, PCM is robust to data disturbs. In addition to its ability to lithographically scale, these characteristics make PCM an attractive NVM for both traditional applications as well as for applications that had previously been beyond the capability of floating gate devices.

At the cell level, the data retention and disturb risk of PCM is primarily confined to the reset, or amorphous phase of the device. This results from the fact that the amorphous state is meta-stable with respect to the stable crystalline phase. Any additional energy applied to this state (via thermal or electrical energy) can accelerate the crystallization process. For data retention, the energy is thermal and provided by the surrounding ambient. There are two types of possible disturbs for the reset state. The first type, known as proximity disturb, can occur in a reset cell if surrounding cells are repeatedly programmed. In this case, the heat generated during the programming operation diffuses from the neighboring cells and accelerates crystallization. The other type of disturb, read disturb, occurs when a device is read many times. This type of disturb is dependent upon the applied cell voltage and ambient temperature.

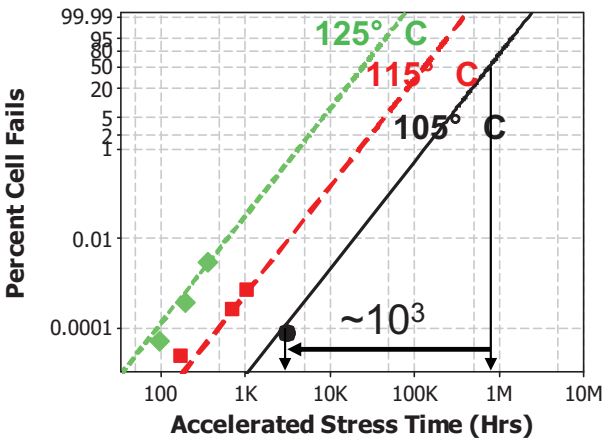

Figure 1. Data from [1] show a 1000x different in failure time between the median (50%) cell and the 1 PPM (0.0001%) cell.

The intrinsic reliability of PCM (as measured in single cells or small arrays) has been shown to be very robust. Cycling counts exceeding 10^{12} have been reported for isolated cells and 10^{9} for fully-integrated cells, and data retention for cells based on $Ge_2Sb_2Te_5$ (GST) is greater than 10 years at 85 °C [3-7]. In addition, read and proximity disturb performance has been shown to be capable of 10 years of continuous reading and 10^{10} writes to surrounding cells [4]. While this intrinsic reliability is a prerequisite, reliability of a memory array is determined by the first instance of either an inability to write new data to the array or read the previously written data without error. For a typical commercial product, the acceptability of such errors is on the order of 100 PPM (parts per million). Considering a 128 Mb array and using the assumption that a single cell failure will result in a product-level error, the acceptable fraction of cell failures during the specified product lifetime is 1 in 10^{12}. However, by employing reasonable usage models and error management schemes this cell failure level can be increased by orders of magnitude. The technology must therefore be assessed based on the earliest failing cells in the distribution at the level required for reliable product operation. The difference between the typical cell and these early failures can be significant. As an example, Figure 1 shows data retention distributions from [7], where the failure time between the median and 1 PPM cell failure time is a factor of 10^{3}. While the majority of PCM publications have not considered PPM-level statistics in their evaluations, several have shown positive results on test arrays [5, 7] and more recently a 4 Mb product based on a 250 nm CMOS technology [8].

90 nm PCM Process Reliability Assessment

In this paper, we present statistical reliability results from a 128 Mb product based on a 90 nm bipolar-selected PCM technology using GST as the memory material, as described in [9-11]. This technology features a 0.097 um^2 cell with a typical programming current of 400 µA (see Figure 2). With optimized programming, this device can achieve a large sensing window between the set and reset states.

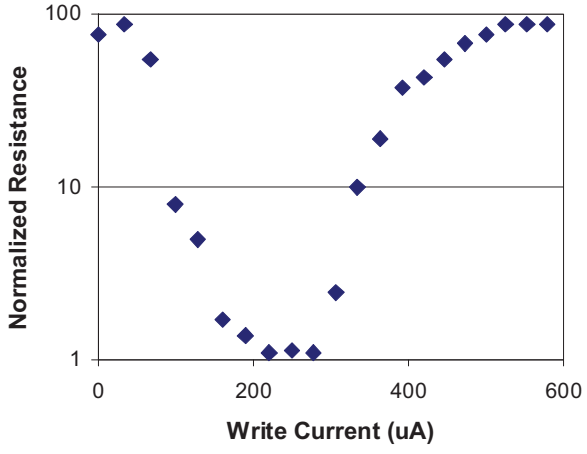

Figure 2. Typical programming curve of a 90nm PCM cell, showing a reset current of 400 µA and a dynamic range of ~100x.

Data retention characterization shows the capability of meeting the 10 yr goal for the technology. As was seen in prior analysis on a 180 nm process technology test vehicle, reduction in the retention early failures requires optimization of both the process integration scheme as well as optimized programming [7]. In addition the activation energy for retention loss (crystallization) remains at 2.6 eV, showing no impact of process scaling.

Cycling endurance is demonstrated to meet 10^{6} writes on a stable basis with proper optimization of the programming algorithm and cell integration scheme. Figure 3 shows the percentage of units passing across a number of lots, where no failures were seen once process and programming improvements were implemented. At the cell level, two modes of cycling

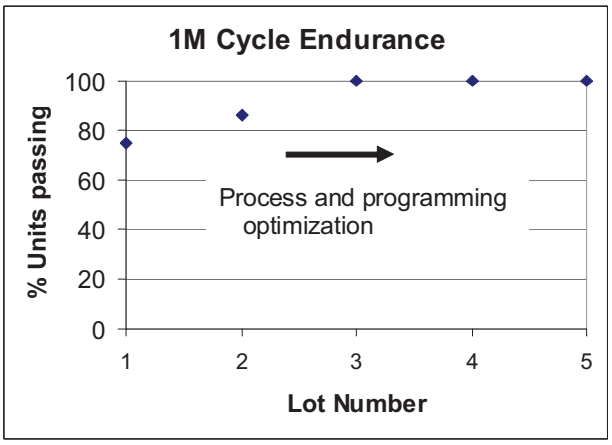

Figure 3. Passing units after 10^6 writes, showing the improvement with process and programming optimization.

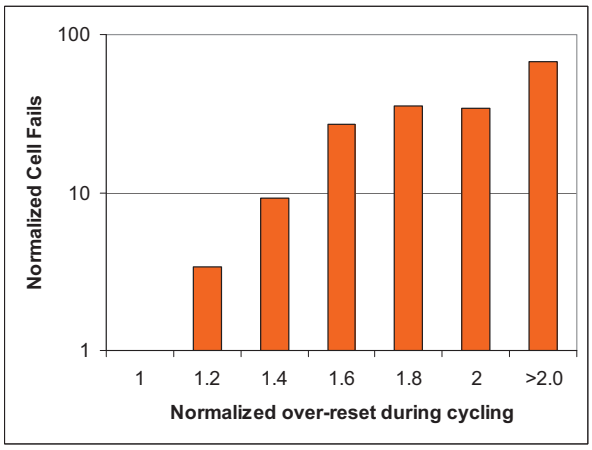

Figure 4. Cell failure rate during cycling as a function of over-reset of the cells.

failures were observed: cell opens ("stuck reset") and reset fails ("stuck set"). Electrical analysis of these cells performed *prior to* cycling showed different signatures for the different types of failures. In general, cells that opened showed a higher threshold voltage than cells that did not fail, suggesting a failure mechanism related to the GST. The reset fails, however, showed matched threshold voltages but a higher resistance in the I-V curve at high current (dV/dI). This suggests that the failure mechanism is related to the heating element. Subsequent physical failure analysis confirmed these hypotheses to be true, showing voiding in the GST above the heater for the open cells and Ge contamination of the heater in the reset fails (which reduced the efficiency of the heater and therefore prevented sufficient melting of the GST). One factor found to be important in PCM programming is the need to use the proper programming currents on the array. Figure 4 shows the relative increase in cell failures with cycles as the amount of over-reset is increased (relative to a cell's optimum reset current). Here we see that a 60% over-reset of the cells gives >10x the number of failures when compared to optimal programming. Furthermore, we find that with optimal programming and process integration we are able to achieve passing results to 10^8 writes. An additional advantage of PCM over floating gate technologies is that cycling a PCM device does not lead to a reduction in data retention. In Flash devices, repeatedly programming and erasing the cell damages the tunnel oxide and reduces the data retention [12]. This mechanism is not present in PCM. Figure 5 shows normalized cell fails after an accelerated retention bake, where we see a reduction in the failing cells with increasing numbers of prior cycles. Measuring the intrinsic retention (with a highly accelerated bake) we find that data retention is slightly improved with writes. This suggests that the chemical composition changes that may take place in the GST during programming (as described in [13] and [14]) do not impact the data retention capability of the device.

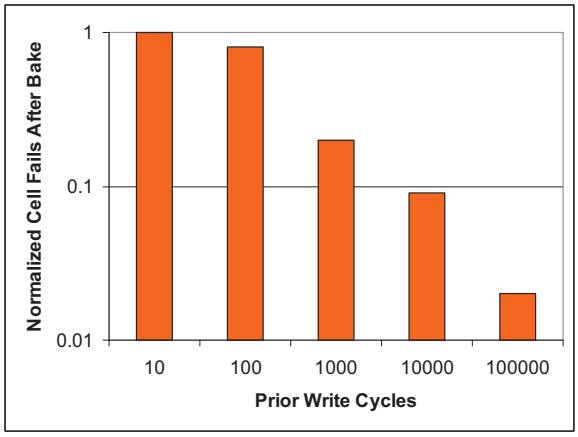

Figure 5. Retention failure rate after an accelerated bake test as a function of prior cycles applied to the array.

Finally, disturb testing shows the technology to be robust to both read and proximity disturbs. Figure 7 shows a distribution of reset cells initially and after 10^{10} reads at non-accelerated conditions. Here we see only the expected drift of cells to higher resistance. Studies at high voltages (still below the threshold voltage) and elevated temperatures show that read disturb is accelerated by both of these parameters. Furthermore, accelerated disturb testing on wafers that were produced with retention optimization in place (that is, the process was

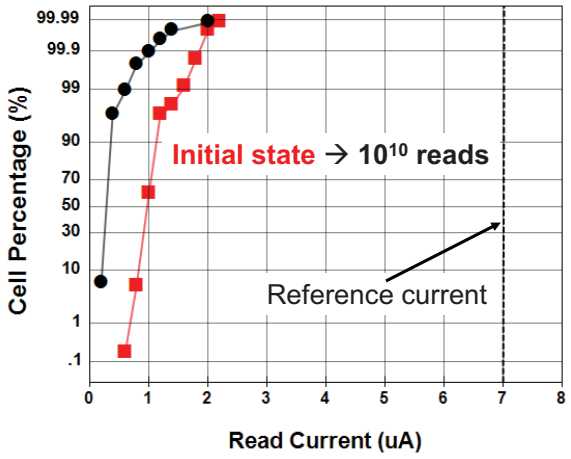

Figure 7. No read disturb (only drift) is observed after 10^{10} reads on reset cells.

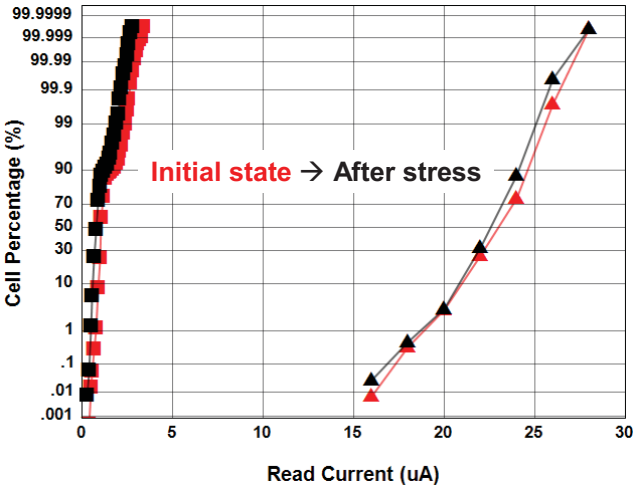

Figure 8. No proximity disturb is seen after stress, which in this case is subjecting the surrounding cells to 10^6 programming operations.

modified to improve data retention) show a corresponding improvement in read disturb. This suggests that the same crystallization mechanism is responsible for both failure modes. Proximity disturb testing was performed by continuously cycling the nearest-neighbor cells to populations of reset and set cells and then checking for any shift in the read current. Figure 8 shows the current distributions both initially and after 10^6 writes to the neighboring cells, where we find only a small amount of drift in the reset cells and no sign of disturb. While only reset cells are expected to be at risk due to crystallization, set cells were included for completeness.

Conclusions

While intrinsic PCM reliability is known to be robust, implementing PCM in large-array devices requires confirmation of reliability to a very low level of defectivity. This requires optimization of both the process integration scheme to reduce variability across cells as well as the programming scheme to minimize damage to cells. With these in place, PCM is capable of high reliability for data retention, cycling endurance, and data disturbs, as demonstrated on a 128 Mb product and 90 nm technology.

References

[1] G. Atwood and R. Bez, "Current status of chalcogenide phase change memory," 63rd Device Research Council Digest, vol. 1, pp. 29-33, June 2005.

[2] S. Eilert et al., "Phase Change Memory: A new memory enables new memory usage models," 2009 IEEE International Memory Workshop, pp. 1-2, May 2009.

[3] S. Lai and T. Lowrey, "OUM – A 180 nm nonvolatile memory cell element technology for stand alone and embedded applications," 2003 IEEE International Electron Devices Meeting, pp. 36.5.1-36.5.4, Dec. 2001.

[4] A. Pirovano et al., " Reliability study of phase-change nonvolatile memories," IEEE Transactions on Device and Materials Reliability, vol. 4, no. 3, pp. 422-427, September 2004.

[5] K. Kim and S.J. Ahn, "Reliability investigations for manufacturable high-density PRAM," 2005 IEEE International Reliability Physics Symposium, pp. 157-162, April 2005.

[6] Ovonic Unified Memory presentation, http://ovonyx.com/technology/technology.pdf

[7] B. Gleixner et al., “Data Retention Characterization of Phase-Change Memory Arrays,” 2007 IEEE International Reliability Physics Symposium, pp. 542-546, April 2007.

[8] J. Rodgers et al., “A 4-Mb Non-volatile Chalcogenide Random Access Memory designed for space applications: Project Status Update,” 2008 IEEE Non-Volatile Memory Technology Symposium, pp. 1-6, November 2008.

[9] F. Pellizzer et al., “A 90nm Phase Change Memory Technology for Stand-Alone Non-Volatile Memory Applications,” 2006 IEEE Symposium on VLSI Technology, pp. 122-123, 2006.

[10] F. Bedeschi et al., “A Bipolar-Selected Phase Change Memory Featuring Multi-Level Cell Storage,” 2008 IEEE ISSCC, pp. 217-227, January 2009.

[11] R. Bez, “Development Lines for Phase Change Memory,” E\PCOS 2008.

[12] R. Bez et al., “Introduction to Flash Memory,” Proceedings of the IEEE, vol. 9, no. 4, pp. 489-502, April 2003.

[13] J. Sarkar and B. Gleixner, “Evolution of phase change memory characteristics with operating cycles: Electrical characterization and physical modeling,” Applied Physics Letters, vol. 91, no. 1, 2007.

[14] S.O. Ryu et al, “Crystallization Behavior and Physical Properties of Sb-Excess $Gs_2Sb_{2+x}Te_5$ Thin Films for Phase Change Memory (PCM) Devices,” Journal of the Electrochemical Society, vol. 153 no. 3, pp. G234-G237, 2006.