Prospect for High-speed, High-density Phase-Change Memory Device with Ge-doped SbTe of a Tuned Composition

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ABSTRACT

Ge-doped SbTe (GeST) of a wide range (~0.7 to ~4.0) of Sb-to-Te ratio (*STR*) was examined with respect to potential use as a material for a high performance phase-change memory (PCM) device. GeST of an *STR* of around 1.8 ($GeST_L$) was found to provide optimal device characteristics in terms of SET speed, RESET current, capability of multi-level storage, and reliability characteristics as well.

Key words: phase-change memory, Ge-doped SbTe, Sb-to-Te ratio

1. INTRODUCTION

GeST's of high Sb contents have received much attention with regard to use as high speed PCM materials because of their very fast growth-dominated crystallization characteristics. In our previous work, GeST of the *STR* of around 4.0 ($GeST_H$) was adopted in a pore-type PCM device to demonstrate markedly shorter SET time (t_{SET}) by about one order than that of $Ge_2Sb_2Te_5$ (GST) [1]. Nevertheless, $GeST_H$-PCM has the apparent drawbacks of high RESET current (I_{RESET}) and inability of multi-level cell (*MLC*) storage. Interestingly, these problems are found to derive by large from fast growth-dominated crystallization kinetics enabling very rapid SET operation otherwise [2]. Reasonably, crystallization kinetics need to be manipulated for optimal device characteristics and this is achievable most effectively by varying *STR* of GeST. Herein, we report about varying programming characteristics of GeST-PCM devices over a wide range of *STR* (~0.7 to ~ 4.0) as well as promising attributes of a PCM with a selected composition *i.e.* *STR* of about 1.8 ($GeST_L$) as a high performance memory.

2. EXPERIMENTS

PCM devices with GeST films of a fixed Ge content of around 10 at% and varying *STR* ranging from ~0.7 to ~4 (refer to a portion of the Sb-Te binary phase diagram in Fig. 1) were fabricated for electrical characterization. As for the device structure, a pore-type was employed where the phase-change material is in contact, through a pore of 150 nm × 150 nm in area, with surface-oxidized *TiN* bottom electrode and is covered with a *TiN* top electrode. The detailed procedures of device fabrication and characterization can be found in ref. [1, 3].

3. RESULTS & DISCUSSION

GeST-PCM devices of varying *STR* were examined with respect to RESET and SET programming characteristics and the results are summarized in Fig. 2 to Fig. 3. From Fig. 2, each of R_{RESET}, R_{SET} and V_{th} appears to decrease rather gradually and continuously with *STR*, similar to a trend displayed by the electrical resistivity data (not shown here). The results for two important performance parameters, t_{SET} and I_{RESET}, are shown in Fig. 2. Notice that I_{RESET} undergoes a rather steep decrease with *STR* decreasing from ~4 to around 1.8 but a markedly slower decrease therefrom to ~0.7. A contrasting trend is observed for t_{SET}, namely a slow increase in the higher *STR* regime but a steep increase in the lower regime. This seems to set *STR* of about 1.8 as an optimum for the best trade-off between t_{SET} and I_{RESET}. From the behavior of crystallization time depicted in Fig. 2 and the fact that *STR* of about 1.8 falls near the Sb-lean end of the δ phase field in the binary Sb-Te phase diagram, we speculate that a qualitative change in crystallization behavior *i.e.* possibly between growth-dominant and nucleation-dominant may come about across *STR*

of around 1.8 so as to affect t_{SET} and I_{RESET} differently in both regimes of *STR*. For the higher *STR* regime where growth-dominant crystallization prevails, we have recently shown that reduction in I_{RESET} with decreasing *STR* can be mostly accounted for by diminished regrowth of crystalline surroundings during melt-quenching. Promising device characteristics of *STR* of 1.8 ($GeST_L$) are summarized in Fig. 4 to Fig. 6. From Fig. 4(a) and 4(b), notice that I_{RESET} of $GeST_L$-PCM is comparable to that of GST-*PCM* while t_{SET} remains much shorter. With regard to reliability, $GeST_L$-PCM shows repeatable RESET/SET operations for more than 10^7 cycles while maintaining an R_{RESET}/R_{SET} ratio of over 100 (not shown). The extrapolated data retention time of $GeST_L$-PCM is around 10 years at the temperature of 117 °C, corresponding to activation energy (E_a) of 3.07 eV (Fig. 5(a)). This is superior to the reported retention characteristics of GST-PCM (10 years at 85 °C, with E_a of 2.1 eV). $GeST_L$-PCM is also shown to have better stability with time *viz.* smaller R_{RESET} drift coefficient than that of GST-PCM (Fig. 5(b)). Finally, multi-level operation (*MLC*) is accomplishable with $GeST_L$-PCM (unlike with $GeST_H$-PCM) by modulated current method as shown in Fig. 6 due to its slower recrystallization rate enabling an effective control of the size of the amorphous region.

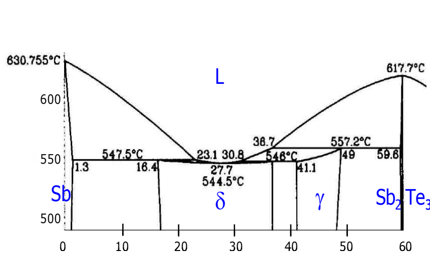

Fig. 1 Equilibrium phase diagram of Sb-Te system

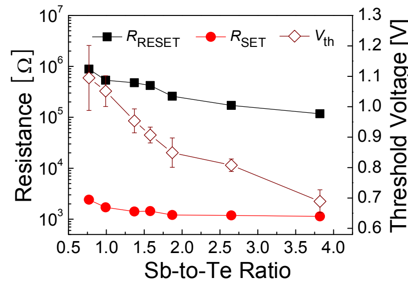

Fig. 2 R_{RESET}, R_{SET} and V_{th} as a function of STR

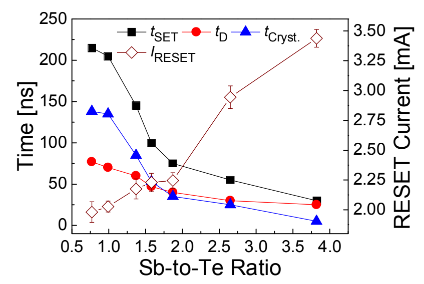

Fig. 3 I_{RESET} and t_{SET} as a function of STR

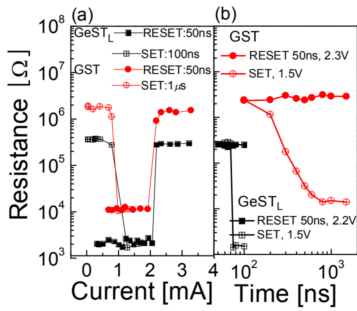

Fig. 4 Comparison of $GeST_L$-PCM with GST-PCM

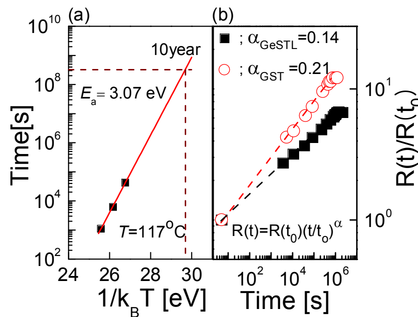

Fig. 5 Data retention and drift characteristics of $GeST_L$-PCM

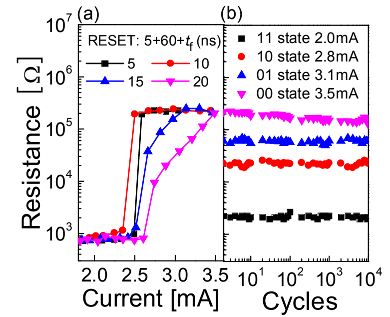

Fig. 6 MLC operation characteristics of $GeST_L$-PCM

4. CONCLUSION

GeST of a lower Sb-to-Te ratio (about 1.8) is a reliable phase-change material of much promise for high speed and high density non-volatile memory application.

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Biographies

Zhe Wu was born in Yanji, Jilin, China, in 1981. He received the B.S. degree in Materials, Mechanical & Automation Engineering from Yanbian University of Science & Technology, China, in 2004, the M.S. degree in Nano-electronics from the University of Science & Technology, Korea, in 2007, and the Ph.D. degree in Material Science and Engineering from Korea Advanced Institute of Science Technology, Korea, in 2010. He also worked as a research assistant in Electronic Materials Center, Korea Institute of Science and Technology from 2005 to 2010 and as a postdoctoral fellow from 2010 to 2011. His Ph.D dissertation was focused on the study of Ge-doped SbTe chalcogenide material for high speed and low power phase-change memory application. Currently, Dr. Wu has joined Samsung Electronics as a senior engineer in new memory division.