Towards Storage Class Memory: access devices using Mixed-Ionic-Electronic-Conduction (MIEC) and modeling of polycrystalline nucleation and growth

Geoffrey W. Burr

IBM Almaden Research Center, 650 Harry Road, San Jose, CA 95120

Tel: (408) 927–1512, Fax: (408) 927–2100, E-mail: *gwburr@us.ibm.com*

ABSTRACT

Memory technology is currently going through a period of rapid change, as new non-volatile memories (NVM) — such as Phase Change Memory (PCM), Resistance RAM (RRAM) and Spin-Torque-Transfer Magnetic RAM (STT-MRAM) — emerge that complement, augment, and potentially could even replace the traditional triad of SRAM, DRAM, and Flash. Storage-class memory (SCM) is an emerging memory category that seeks to combine the benefits of solid-state memory, such as high performance and robustness, with the long-term retention and low cost of conventional hard-disk magnetic storage.

However, such SCM technologies will require large nonvolatile memory arrays that can be manufactured at a very low cost per bit. One path to this goal is to stack multiple layers of NVM crosspoint arrays in 3D. In such an architecture, the NVM element at each crosspoint intersection must be in series with an access device, whose strong nonlinearity makes it possible to drive high current density through selected cells while maintaining ultra-low leakage through unselected cells. 3D stacking is only possible if both the NVM and the access device are fully compatible with a Back-End-Of-the-Line (BEOL) fabrication process.

In PCM, grain boundaries in the phase change material affect all resistance device states yet have not been widely studied. We have studied the formation of fcc polycrystalline grains from the as-deposited amorphous state in undoped Ge2Sb2Te5, performing ex situ transmission electron microscopy membrane experiments and then matching those observations against numerical simulations using classical nucleation theory.

This talk will combine a review of our work on modeling of nucleation in PCM materials together with a review of our novel access devices based on Cu-containing Mixed-Ionic-Electronic-Conduction (MIEC) materials. Such MIEC-based access devices not only meet all of the necessary requirements but also support the bipolar memory operation critical for NVM candidates such as RRAM and STT-MRAM. Experimental results will be shown, including cycling endurance, array fabrication and yield, integration with PCM, speed, and scalability.

Key words: Access device, MIEC, PCM, NVM, RRAM, MRAM

1. ACCESS DEVICES USING MIXED-IONIC-ELECTRONIC-CONDUCTION

Cost-effective 3D-stacking of large crosspoint arrays in the Back-End-Of-the-Line (BEOL) requires either a selection device with very large ($>10^6$) non-linearity (Fig. 1), or an NVM device which itself possesses such non-linearity. An Access Device allows a choice of crosspoint-array voltages such that the selected device passes the desired current (either for read or write) while both the myriad *unselected* devices generate ultra-low leakage and the numerous *half-selected* devices along the same selected bit- or word-lines generate modest amounts of leakage (Fig. 2). The larger such arrays can be made, the lower the overhead from peripheral circuitry — and thus the higher the efficiency in terms of accessible bits per unit area of silicon.

BEOL-friendly access devices (ADs) based on Cu-containing MIEC materials [1-5] have become an intriguing choice as 3D-ready selection devices for Non-Volatile Memory (NVM). Beginning in 2010, our group at IBM Research – Almaden has showed that such MIEC-based ADs offer the large ON/OFF ratios, high voltage margin V_m (over which current $<$ 10nA), and ultra-low leakage ($<$10pA) needed to enable large arrays, as well as the high current densities needed for PCM and the fully bipolar operation needed for high-performance RRAM [1,2]. We have shown that MIEC-based ADs can be

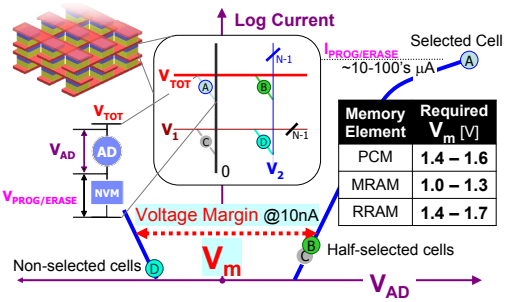

Fig. 1 In an NVM crosspoint array, the Access Device (AD) must supply high current for program/erase of a selected cell yet low-leakage for all other cells, including those half-selected. A voltage margin V_m of 1.5V would be sufficient for PCM, RRAM, and MRAM.

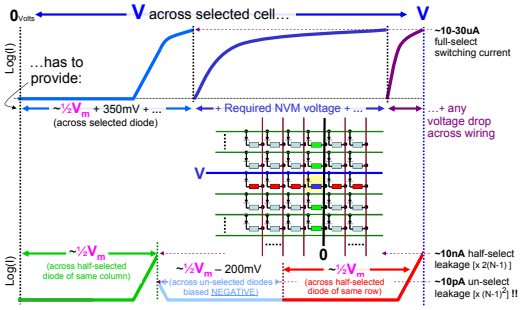

Fig. 2 Voltage on a selected NVM+AD affects 3 other sets of ADs: those in the same row, in the same column (both *half-selected*), and all others (*un-selected*). Each AD must hold ultra-low (∼10pA) leakage for hours, maintain modest (∼10nA) leakage for seconds, and occasionally pass either read-level (3-6uA) or write-level (30-60uA) currents.

integrated at 100% yield (at 512kBit scale) [3], can provide write-level (>100uA) currents within 15ns [3], and can be scaled to the <30nm CDs and <12nm thicknesses found in advanced technology nodes [4]. Most recently, we have demonstrated that MIEC-based ADs can sustain and move rapidly between *un-selected, half-selected, selected-for-read*, and *selected-for-write* states [5]. Thus ultra-low leakage can be maintained over hours, leakage recovery after write (30-50uA) operations requires ∼1us (with read (3-6uA) recovery even faster), and read operations can be fast enough for use with MRAM (sub-50ns) [5]. Inherently-fast thin MIEC ADs offer similar speeds at modest overvoltages (for minimal read disturb) [5].

Our MIEC-based ADs are integrated on 8" wafers, with Cu-containing MIEC material sputtered into vias followed by an optimized CMP process [2] and a confined, non-ionizable TEC. Conductive-AFM testing of short-loop devices with minimal wiring has validated single-target deposition and revealed a wide processing temperature window (up to 500°C) for these MIEC-based ADs [3].

Bi-directional Array Diagnostic Monitor (ADM) arrays up to 512×1024 integrated MIEC ADs have been tested using integrated 1-bit sense-amplifiers and a fast electrical tester (Magnum 2EV) [3]. Cumulative distribution functions (CDFs) of the bitline voltage V_{BL} needed to produce various device currents I_d show the tightly distributed array I-V characteristics (Fig.3(a)). All 524,288 MIEC devices — 100% — had $V_m > 1.1$V, and 99.955% of ADs fell within ±150mV of the median voltage margin V_m=1.36V at 10nA (Fig.3(c)) [3].

Thickness scaling experiments showed that as MIEC-based ADs become thinner, voltage margin remains mostly unchanged until the minimum gap between electrodes, d_{min}, reaches ∼11-12nm [4]. Short-loop MIEC ADs fabricated with ultra-scaled vias show both high yield and high voltage

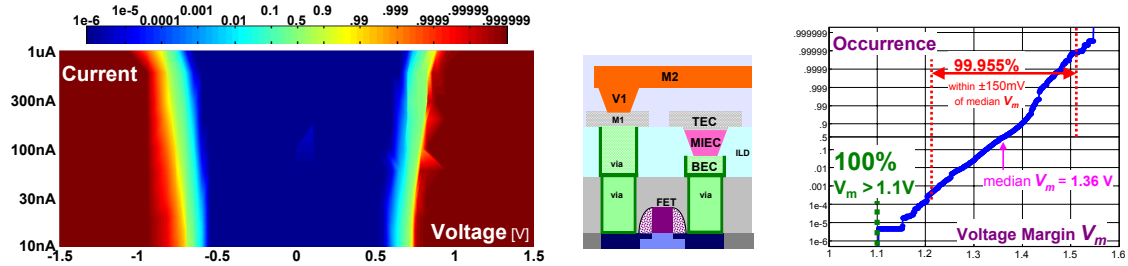

Fig. 3 Cumulative distribution functions (CDFs) across bitline voltage V_{BL} at various device currents I_d (a) show array level I-V results with tight distributions across a 512×1024 array of (b) integrated MIEC ADs . (c) Within this same 512×1024 array, there were no leaky devices; 100% of the array showed $V_m > 1.1$V, while 99.955% of MIEC ADs had voltage margins V_m at 10nA within ±150mV of the median of 1.36V.

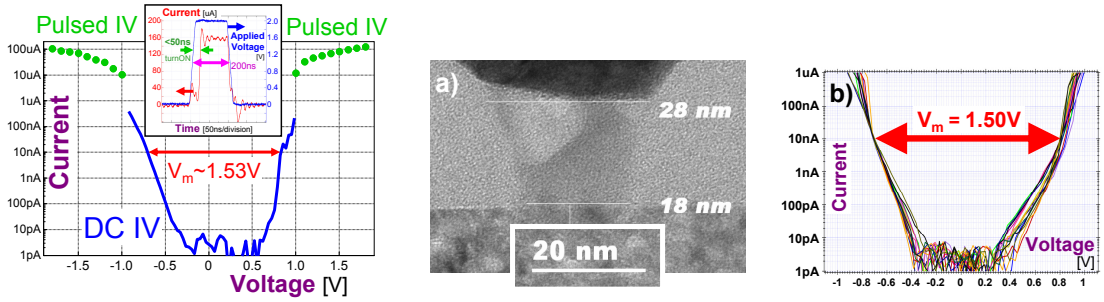

Fig. 4 (a) In addition to high yield, scaled short-loop MIEC ADs exhibit the same >1e7 ON-OFF contrast, <50ns turn-ON times (test-setup-limited), and ultra-low leakage shown previously [2,3] in larger devices. Aggressively-scaled short-loop MIEC ADs[3], with (b) both TEC and BEC <30nm, show (c) large voltage margins and ultra-low leakage[3,4].

margin[4]. Despite their small size, these MIEC ADs can still rapidly drive the large currents needed for NVM switching (Fig.4(a)). Voltage margin V_m (at 10nA) improves markedly as devices are scaled in lateral size. Aggressively-scaled MIEC ADs retain all requisite characteristics, including ultra-low leakage (<10pA) and the large voltage margins (V_m > 1.50V) needed for large arrays, even with both top and bottom CDs <30nm (Fig.4(b,c)). Unlike thickness scaling, where leakage increases sharply for $d_{min} \sim$ 6nm, no lower limit to CD scaling has yet been identified[4].

Integration of MIEC ADs immediately above small (CD∼35nm) PCM devices allowed testing of integrated PCM+MIEC device pairs. Fig. 5 demonstrates endurance in excess of 100,000 cycles, despite the repeated application of RESET pulses >200μA and 5μs long SET pulses at ∼90μA [3]. To demonstrate NVM write speed capabilities, an MIEC-based AD was used to rapidly RESET a co-integrated PCM device. After each 15ns RESET pulse at varying amplitude (Fig. 6(a)), a long SET pulse recrystallized the doped-$Ge_2Sb_2Te_5$ PCM material. After each pulse, bipolar dc IV curves (Fig. 6b,c) showed the expected change in the PCM resistance above the same low-leakage characteristics of the MIEC AD [3]. The application of shaped pulses or a transient "overvoltage" read readily allows MIEC ADs to support ∼5uA NVM reads in <50nsec [4,5].

2. MIEC: CONCLUSIONS

BEOL-friendly access devices (AD) based on copper-containing MIEC materials [1-4] uniquely enable multi-layer crosspoint-memory arrays, offering the large currents (>100uA) needed for PCM, the bipolar operation required for high-performance RRAM, single-target sputter deposition, ultra-low leakage (< 10 pA) and high voltage margin (1.5V) [3]. Co-integration with PCM [3], integration in large (512×1024) arrays with 100% yield [3], and tight distributions, fast transient operation [3,5], long-term persistence of the required ultra-low-leakage [5], and scalability to aggressive technology

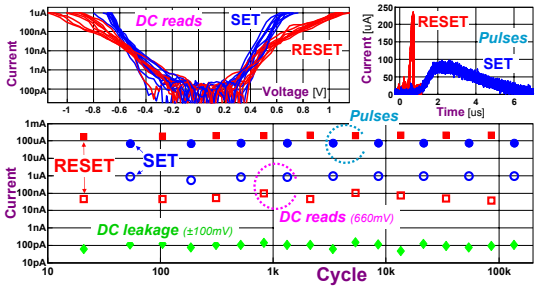

Fig. 5 Endurance of an integrated PCM+MIEC device-pair to >100k cycles, with RESET currents >200μA and 5μs-long SET pulses (∼90μA). No AD degradation or PCM failure had occurred at the time testing was terminated.

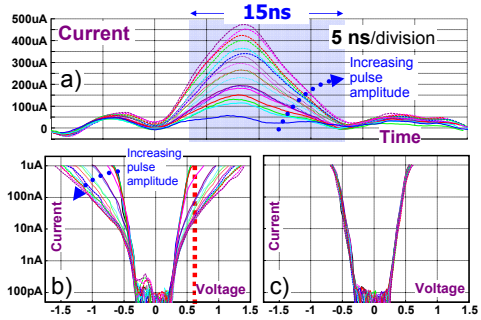

Fig. 6 Unlike PCM SET (limited by crystallization), RESET occurs as rapidly as (a) the co-integrated MIEC AD can supply sufficient switching current. After each pulse, bipolar dc IV curves demonstrated the large resistance contrast (∼1MΩ) between (b) PCM RESET and (c) SET states; despite the large currents, the low-leakage characteristics of the MIEC AD remain unaffected.

nodes has been demonstrated[4].
Thus MIEC-based ADs are well-suited for both the scaled CDs and thicknesses of advanced technology nodes and the fast read and write speeds of emerging NVM devices. Future work includes a better quantitative understanding of the interaction between the mobile Cu-ion dopants and the resulting electronic current, improvements in endurance at high current (currently $\sim 10^8$ cycles at 150uA [2]), and increases in the voltage margin so as to enable large arrays for NVM devices requiring $>$1.5V switching voltages.

3. SIMULATIONS OF NUCLEATION AND GROWTH IN $Ge_2Sb_2Te_5$

The relationship between the polycrystalline nature of phase change materials (such as $Ge_2Sb_2Te_5$) and the intermediate resistance states of phase change memory (PCM) devices has not been widely studied. A full understanding of such states will require knowledge of how polycrystalline grains form, how they interact with each other at various temperatures, and how the differing electrical (and thermal) characteristics within the grains and at their boundaries combine through percolation to produce the externally observed electrical (and thermal) characteristics of a PCM device.
We have addressed the first of these tasks (and introduced a vehicle for the second) by studying the formation of fcc polycrystalline grains from the as-deposited amorphous state in undoped $Ge_2Sb_2Te_5$ [6]. We performed *ex situ* Transmission Electron Microscopy (TEM) membrane experiments and then matched these observations against numerical simulation.
Our numerical simulator — which models nuclei formation through classical nucleation theory and then tracks the subsequent time– and temperature–dependent growth of these grains — can match these experimental observations of initial grain distributions and crystallization temperature both

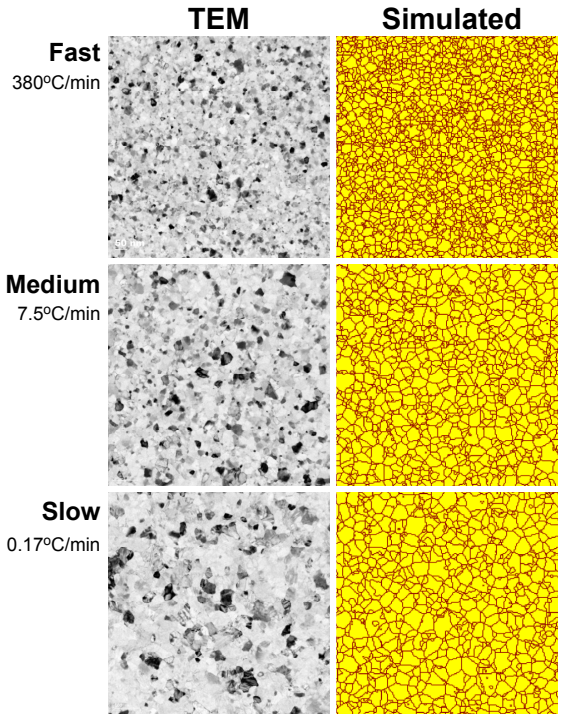

Fig. 7 TEM (Transmission Electron Microscopy) (left) and simulated (right) grain images for three different ramp-rates (380, 7.5 and 0.17°C/min). All images are shown at the same scale, each corresponding to an area of 886nm × 886nm. In the grain images from our classical nucleation theory simulator, yellow represents a crystalline voxel and brown a grain boundary.

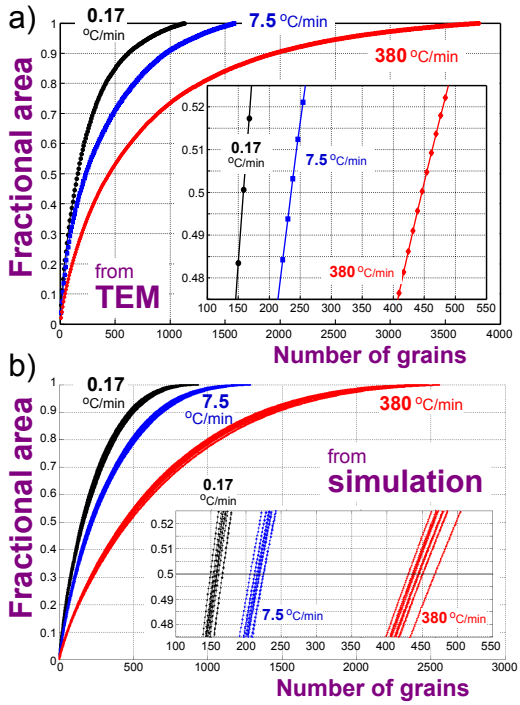

Fig. 8 Cumulative distribution of area covered by polycrystalline grains, from largest to smallest, according to image analysis of a) the TEM images from Fig. 7 and b) the grain sizes obtained directly from simulation. For each simulated ramp-rate, ten different simulations with different random seeds were run. Large grains will lead to a steep curve, while numerous small grains will result in a much more gentle curve.

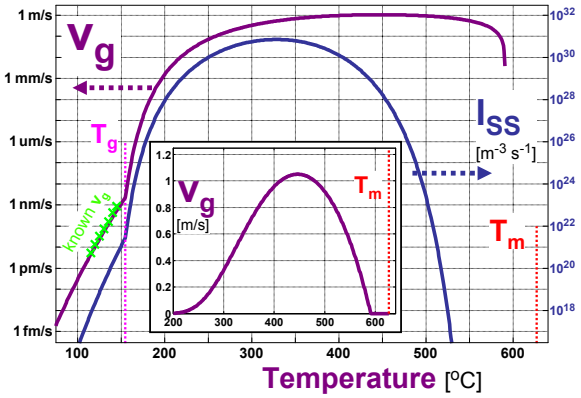

Fig. 9 Crystal growth velocity, v_g, and steady-state nucleation rate, I_{ss}, as a function of temperature. The inset replots v_g on a linear scale in the high temperature regime. Both the melting temperature T_m and glass transition temperature T_g are shown. Symbols at lower left show low-temperature crystal growth velocities obtained experimentally with AFM measurements[8].

qualitatively and quantitatively. This simulator was originally developed to help track distributions of sub-critical nuclei, as observed by Fluctuation-TEM and optically-induced crystallization of pre-annealed (primed) and un-primed GST samples[7].

Ramped-anneal experiments show that the temperature ramp-rate strongly influences the median grain size. The left side of Fig.7 shows grain distributions as indicated by bright-field TEM imaging through three TEM membranes after ramped–anneals at widely varying rates, ranging from 380°C/min down to 0.17°C/min. The right side shows simulated grain distributions for the same ramp-rates, with yellow representing a crystalline voxel and brown a grain boundary. The pixels are plotted in such a way that even a single-voxel polycrystalline grain would result in one yellow pixel surrounded by a ring of brown pixels.

In order to quantify the grain size distributions in these images, we tabulated the grain areas for each TEM and simulation image, and plotted these as a cumulative distribution function — e.g., fraction of area covered as a function of the number of grains (Fig.8). Although these plots all rise monotonically, an image with a few large grains will be associated with a very steep grain-CDF curve, while an image with many small grains will give rise to much more gentle CDF. The "median" grain-size — the inverse of the slope of each curve as it passes through 50% — is such that half of the area is covered by larger grains, and half by smaller grains.

By truncating similar ramped-anneal experiments at various peak temperatures, we convincingly

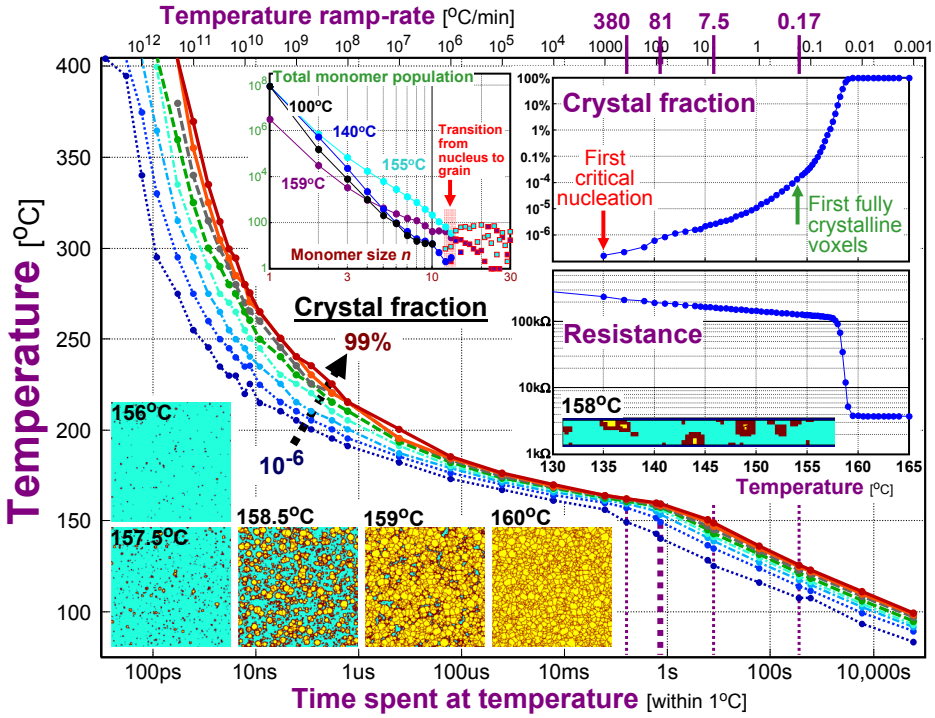

Fig. 10 Crystal growth velocity, v_g, and steady-state nucleation rate, I_{ss}, as a function of temperature. The inset replots v_g on a linear scale in the high temperature regime. Both the melting temperature T_m and glass transition temperature T_g are shown. Symbols at lower left show low-temperature crystal growth velocities obtained experimentally with AFM measurements[8].

demonstrated that the temperature range over which these grains are established is quite narrow. Subsequent annealing at elevated temperature appears to change these established distributions of grain sizes only slightly [6]. Temperature ramp-rate strongly influences the median grain size because of the difference between the exponential temperature dependence (activation energies) of crystal growth velocity v_g and nucleation rate I_{ss} below the glass transition temperature T_g (Fig. 9). The grain dependence arises because of the temperature at which the bulk of the crystallization occurs, and in turn, which particular temperature dominates the crystallization then depends on the ramp rate. These simulations show that the particular narrow temperature range over which crystallization occurs shifts as a function of temperature ramp-rate, which allows us to quantify the lower portions of the Time-Temperature-Transformation (TTT) map for $Ge_2Sb_2Te_5$ (Fig. 10).

4. NUCLEATION AND GROWTH: CONCLUSIONS

We have studied the formation of fcc polycrystalline grains from the as-deposited amorphous state in undoped $Ge_2Sb_2Te_5$ (GST), by combining $ex\ situ$ Transmission Electron Microscopy (TEM) membrane experiments with numerical simulation. Our numerical simulator was able to match these experimental observations of initial grain distributions and crystallization temperature both qualitatively and quantitatively.

This work represents a first step towards understanding the crucial relationship between the polycrystalline nature of phase change materials and the intermediate resistance states of phase change memory (PCM) devices, with impact on long-term data retention, predictable device operation, and long-term resistance drift. Future experiments include extensions of the simulator to investigate temperature-dependent interactions between neighboring grains, and to study nucleation from within the melt-quenched amorphous state.

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Biography:

Geoffrey W. Burr received his Ph.D. in Electrical Engineering from the California Institute of Technology in 1996 under the supervision of Professor Demetri Psaltis. Since that time, Dr. Burr has worked at the IBM Almaden Research Center in San Jose, California, where he is currently a Research Staff Member. He has worked in a number of diverse areas, including holographic data storage, photon echoes, computational electromagnetics, nanophotonics, and computational lithography. Dr. Burr's current research interests include non-volatile memory, reprogrammable logic, and cognitive computing. A Senior Member of IEEE, Geoff is also a member of MRS, SPIE, OSA, Tau Beta Pi, and Eta Kappa Nu.