New Materials for Low-Power PCM for Storage Device Applications

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ABSTRACT

We report on phase change memory (PCM) research from the Low-power Electronics Association and Project (LEAP) that aims to develop non-volatile memories (NVM) for next generation storage devices. We present a new development of GeTe/Sb_2Te_3 super-lattice PCM materials and Nano-GST materials for low-power, low-voltage, and high-endurance operation.

Key words: PCM, GeTe/Sb_2Te_3 super-lattice, Nano-GST.

1. INTRODUCTION

'Big data' are various kinds of data that have been generated with the diffusion of the Internet and the development of IT technologies. The needs for storing and utilizing these data are growing. It is anticipated that the bit capacity of desk storage in data centers in 2020 will become 45 times larger than the bit capacity in 2011. In addition, the need for storage systems which consume a low amount of power and process at high speed have stimulated the spread of solid state drives (SSDs). While FLASH memories are widely used as semiconductor non-volatile memories (NVMs) in SSDs, next generation SSDs requires NVMs with lower power consumption and higher speed operation than those of FLASH memories. This is especially the case when using SSDs in the highest level of the storage system hierarchy. Phase Change Memory (PCM) is a possible next generation non-volatile memory. The data rate of an SSD with PCM is expected to be much faster than that with NAND FLASH memory. The chips with a faster data rate will result in a reduction in both the power and the number of chips needed in an SSD (Fig. 1). The data rate after 2018 will be satisfied by using new PCM materials with power consumption of less than 1/10 that of conventional phase change materials. We report on new materials of GeTe/Sb_2Te_3 super-lattice (SL) structure [1][2], and Nano-GST[3] as solutions for reducing the power consumed by PCM for storage device applications.

2. GeTe/Sb_2Te_3 Super-Lattice Phase Change Memory

The GeTe/Sb_2Te_3 SL structure has been investigated extensively by J. Tominaga, et al. In the SL structure, a movement of Ge atoms is the main cause of resistance change. Theoretically, less than 1/20 of bit programming energy is required than that for the crystal-amorphous phase change in $Ge_2Sb_2Te_5$ alloy materials. In this work, we developed process technologies and measured the electrical properties of GeTe/Sb_2Te_3 SL memory cell in-line with a 300-mm Si wafer. Eight cycles of the GeTe/Sb_2Te_3 periodic unit were deposited using physical vapor deposition (Fig. 2). The crystal structure of SL films was clarified to have an XRD peak characteristic to SL films. A pulse R-I curve of SL in set and reset operations is shown in Fig. 3. The diameter of the BE contact was 50 nm. The set resistance was about 1 k Ω and the reset resistance was more than 1 M Ω. The set current was 60 uA, and the reset current was 1 mA. The endurance of $>1 \times 10^6$ cycles was obtained with the set/reset resistance ratio of more than 100. The SL PCM will make low-power and high-data rate solid state storage devices in the next generation.

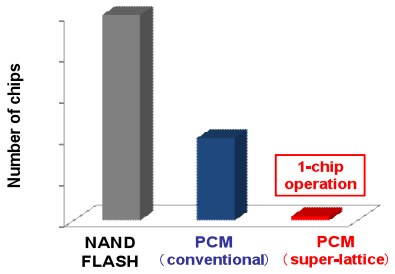

Fig. 1 Number of chips for 1000 MB/s SSD operation.

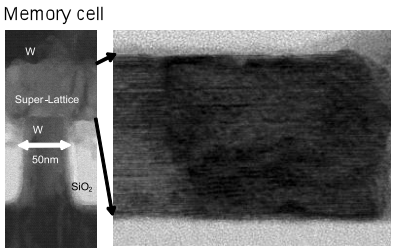

Fig. 2 $GeTe/Sb_2Te_3$ Super-lattice PCM.

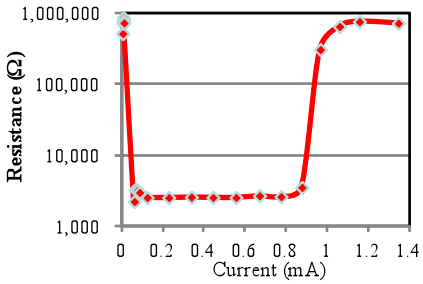

Fig.3 R-I curve of $GeTe/Sb_2Te_3$ Super-lattice PCM.

3. Nano-GST

We have demonstrated the advantages of Nano-crystalline doped-$Ge_2Sb_2Te_5$ with low thermal conductivity, κ. Device simulations showed a thin layer with high resistivity, ρ, and low κ could be used to suppress heat dissipation through the plug. To control κ and ρ, we investigated compositization by using a combinatorial co-sputtering deposition method, and investigated composite of the $Ge_2Sb_2Te_5$ (GST) and a dielectric material. Thanks to a nano-crystalline structure, the thermal conductivity of GST+10%Dielectric (referred to as Nano-GST) dropped below those of elemental GST and Dielectric. Nano-GST enabled 68% lower reset current, 0.33mA, which was 1/3 of a conventional GST, and 90% reset power reduction, 3.6 pJ, which was 1/10 of conventional GST. High crystallization temperature (~ 215 ºC) and endurance of $>1\times10^7$ cycles were obtained. Nano-crystalline GST is a promising material for low-power phase change memory.

4. CONCLUSIONS

We have demonstrated excellent properties of low-power $GeTe/Sb_2Te_3$ super-lattice and Nano-GST PCM. The SL memory cells were fully fabricated in line with a 300-mm Si wafer and showed excellent device performance such as the lowest set current ever reported. Nano-GST with low thermal conductivity was synthesized and had a reset energy of 3.6 pJ. The SL and Nano-GST PCM will be used to make low-power and high data-rate solid state storage devices in the next generation.

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