Engineering of Programming Operation for Increased Performances in Non Volatile Phase Change Memory

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ABSTRACT

Non Volatile Phase Change Memory for embedded applications is now entering in an industrialization phase at 90nm technology node. This requires to implement customization both on process and programming algorithm side to better fit different applications. In this work in particular we focus on the engineering of the programming operation for conventional $Ge_2Sb_2Te_5$, to take into account different constraints in terms of speed and power and/or to improve reliability performances. We show that a "single shot" approach is a viable solution to program multi-megabit arrays. Moreover, pulse shape and amplitude can play a relevant role for both reading window opening and improved endurance.

Key words: phase change memory, set pulse speed, endurance

1. INTRODUCTION

The full integration of a 4Mb ePCM macrocell with three additional masks and minor process tuning has been demonstrated and confirmed as a viable solution for floating gate non-volatile memory replacement in embedded applications [1]. Aim of this work is to present the engineering of the programming operation. It is well known that Reset pulse amplitude is defined by cell architecture and reliability constraints, since proper amorphous dome is needed to guarantee retention. So, we focused on the optimization of the Set pulse to minimize the associated energy, with no drawback on active performances [2]. Final target is to find the best trade-off in terms of speed for high writing throughput, energy consumption for high parallelism and low power operations. The outcome of this characterization is a large reading window on 4Mb and enhanced endurance at cell-level.

2. EXPERIMENTS

Electrical characterization has been performed at the level of analytical cell and whole array. Reference process is a 90nm 6 Metal Level logic platform, with a Wall-like PCM cell integrated after plug definition [1]. Phase Change material is conventional $Ge_2Sb_2Te_5$ and the array of 4Mb Test Chip is built by MOS-selected PCM cells [3].

3. RESULTS & DISCUSSION

Set pulse optimization has been addressed in 3 steps: slope, cut-off and amplitude.

In order to evaluate the Set speed of electrically activated $Ge_2Sb_2Te_5$ (the so called GST), the quenching time needed to reach the minimum Set resistance has been measured. After a Reset pulse corresponding to the highest resistance value (Fig.1), a triangular Set pulse with fixed amplitude (same as Reset) and an increasing trailing time from hundreds of ns to few µs has been applied. After each Set pulse the low field resistance is measured as function of the trailing time (Fig.2). The best Set state is obtained with a minimum quenching time of 400ns, giving a trailing slope of about -1µA/ns.

A further optimization of the Set pulse can be obtained by playing with the introduction of a cut-off current level. The purpose is to shorten the Set pulse as much as possible with no degradation of the final Set resistance, since

during the trailing slope the temperature inside the active portion of GST sweeps down from melting temperature. A specific I_{cut} current level can be determined, whose value must be kept below I_{melt} (Fig.3).

Concerning Set pulse amplitude, first experiment was performed with reference condition $I_{Set}=I_{Reset}$. Different current levels have been considered above and below Reset saturation condition (Fig.1) and a very small impact on the finally achieved Set and Reset resistance values has been observed (Fig.4, blue dots).

Next step is the evaluation of the Set efficiency as a function of the Set pulse amplitude, by keeping the Reset current above saturation value (over-reset condition). A good final Set state can be achieved by significant lowering of the current amplitude (I_{set}) in the range of $I_{Reset}/2$ (Fig.4, red dots). The net outcome is a Set pulse which can guarantee very good final state and low power consumption with positive feedback on write throughput.

In Fig.5a we demonstrate that proper Set pulse engineering has an impact also on cell cycling performances. Several experiments have been performed by considering different pulse shape and amplitude. End-of-life cycling experiments showed that programming through a low current Set pulse can improve endurance by one order of magnitude (roughly from 30Mcycles to 300Mcycles). Moreover, main impact on cycling performances is due to the current peak applied rather than the total amount of energy associated to the Set pulse (Fig.5b).

Concerning the behavior of large arrays, we demonstrated that a “single shot” approach with no need of complex recovery algorithm is a viable solution for 4Mb PCM Test Vehicle (Set and Reset distributions in Fig.6 – blue curves). The low current approach for the Set pulse found effective for cell endurance is feasible also for the multi-megabit array. In this case a slower pulse slope is needed to recover tail bits of the Set distribution (Fig.6 – red curve).

4. CONCLUSION

An engineering of the Set programming pulse has been presented in terms of pulse shape and related energy. It has been shown that there is room to improve PCM programming according to specific application needs. We proposed for 90nm ePCM technology based on $Ge_2Sb_2Te_5$ an optimized Set pulse. Effectiveness for programming has been demonstrated both at cell-level and on 4Mb Test Vehicle. Finally, improved endurance properties have been obtained with this optimized Set pulse.

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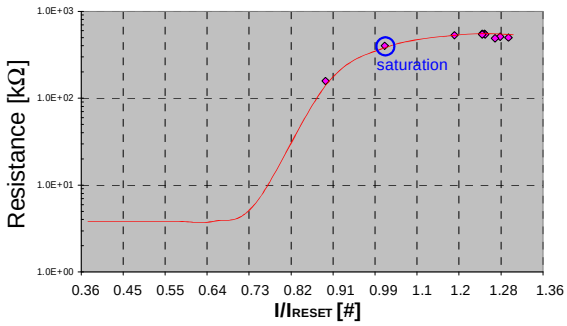

Fig.1: R – I plot of a typical PCM cell where the Reset saturation condition and other over/under-reset condition explored in this characterization are highlighted.

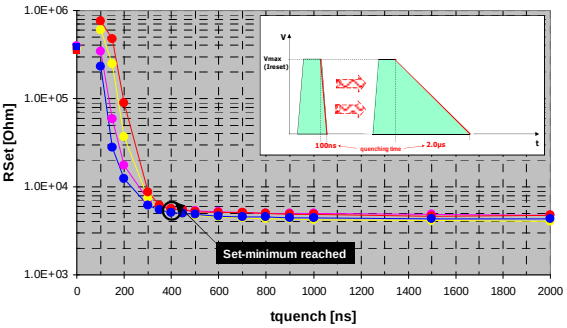

Fig.2: Set speed characterization performed on analytic cell where the Set resistance is plotted as function of the quenching time.

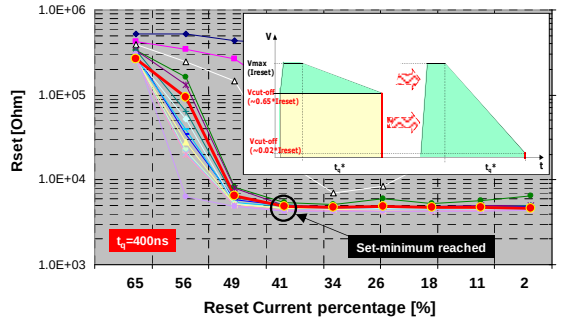

Fig.3: Set pulse optimization performed on analytic cell where Set resistance is plotted as function of the cut-off current considered. Focus is on the fastest quenching time found so far (red curve): best I_{cut}~0.4I_{Reset}.

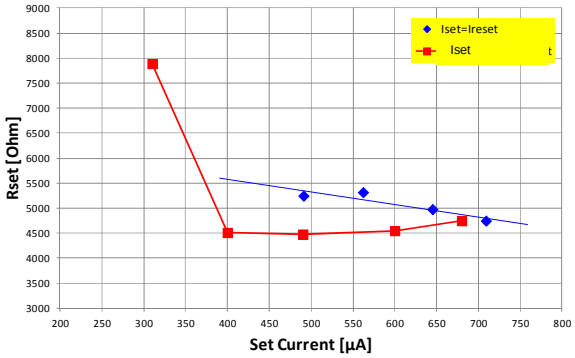

Fig.4: Slight dependence on pulse height with the approach I_{Reset}=I_{Set}, while with I_{Reset} in over-reset condition good Set resistance achievable even with I_{Set} in the range of I_{Reset}/2.

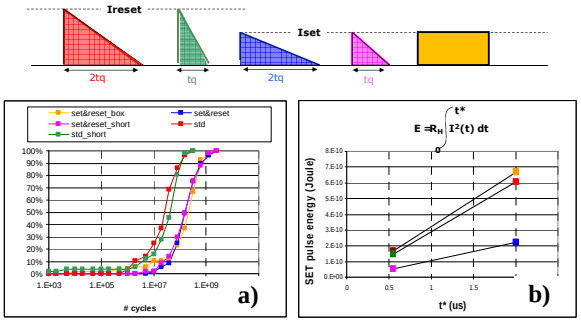

Fig.5: Cycling with a low current Set pulse allows to increase the cycles by 1 decade (a). Energy calculation of different Set pulses shows that main endurance detractor is current peak rather than total amount of energy supplied to the cell (b).

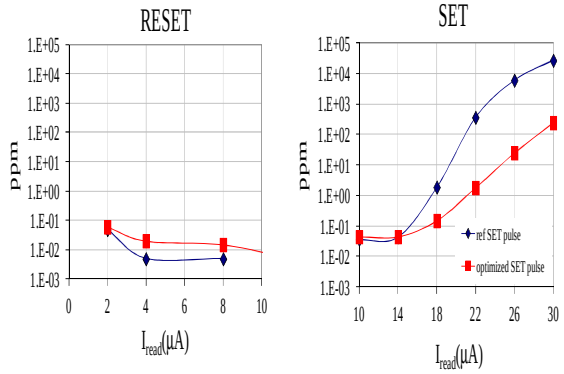

Fig.6: Reset and Set (cumulated on wafer) distribution collected on 4Mb ePCM Test Vehicle: the low current Set pulse with optimized (slower, in red) slope is effective to improve the distribution.