Multi-levels phase change memory using pulse modulation

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ABSTRACT

We will describe pulse modulation for multi-levels lateral type (ML-) phase change memory (PCM). In order to use the ML-PCM as a random access memory (RAM), we have to develop a method to control the resistance from high to low or from low to high value for the memory access free. We have proposed ML-PCM using current control and 2-steps-pulse with various 2nd pulse width like a stair-case as one of pulse modulations for decreasing and increasing the resistance, respectively. We demonstrate that the crystalline and amorphous regions are controlled using the current control and the pulse modulation, respectively, theoretically and experimentally.

Key words: multilevel PC recording, PC resistance control, GeSbTe, SbTe, PC simulation.

1. INTRODUCTION

Recently, electronic devices need many nonvolatile memories for easy and fast operation of them and decrease of consumptive power. In order to use the multi-levels-phase change memory (M-PCM) as a random access memory (RAM), we have to develop a method to control the resistance from high to low and from low to high value for the memory access free. We have proposed multilevel lateral type (ML-) PCM using current control and 2-steps-pulse control with the 2nd pulse width like a staircase as one of pulse modulations for decreasing and increasing the resistance for the multi-levers recording, respectively. Many M-PCMs have been proposed[1-4]. The multilevel recordings can be selected mainly to 2 type methods such as controlling the resistance with length of amorphous region and cross section of crystalline region in amorphous region.

We have developed the ML-PCMs using stacked PC and heater layers[4] and controlling the cross section of crystalline region[3]. The controlling the cross section can change the resistance from high to low value. In the process, filament path occurs at first and crystalline region expands following heating based on the filament path. The multi-levels control was achieved with current control. However, it is very difficult to change the crystalline region to amorphous region by the same control. In order to change the resistance from low to high value, we have proposed 2-steps pulse application

with both amorphization and crystallization processes[5]. The method is one of pulse modulations. The technique has been applied to precise writing in digital versatile disk (DVD) optical recording with laser pulse modulation. The plural steps pulse recording has also been introduced in multi-levels PCM by T. Nirschl et al.[1]

In this research, the crystallization is achieved by controlling the annealing time in these process. We have studied the possibility to do random access writing in multi-levels PCM using the pulse modulation theoretically and experimentally. Especially, it is very interested that we study the control of the resistance from low to high value in crystalline state passing the amorphous state by the pulse modulation. We describe multilevel recordings for decreasing and increasing the resistance using the current control and the pulse modulation, respectively.

2. SIMULATIONS

The device model was used with lateral type PCM with a top heater as shown in Fig. 1[6]. The simulation executed 2 ways to control the resistance from high to low and from low to high value by applying the pulse between the TiN electrodes.

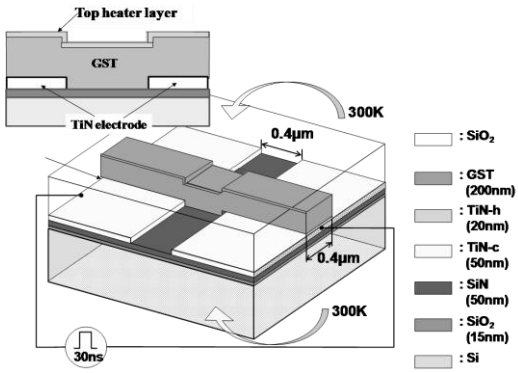

Fig. 1 Simulation model of device structure for FEM method.

2. 1 Decrease of the resistance from amorphous state

When applying the pulse to the electrodes, the electric field exceeds critical field of about 38 V/μm and 15 V/μm in $Ge_2Sb_2Te_5$ and SbTb, respectively[4]. Then, some filament paths appear in the phase change (PC) material. The current starts to flow between the electrodes and the temperature increases rapidly. The crystallization of the amorphous state is accelerated by keeping the temperature between the crystallization point and melting point. Figure 2 shows a scheme of the crystallization mechanism, a variation of the temperature and a current-voltage (resistance) property of the device. Over the critical field, the current increases and the power puts into the PC material. Figure 3 shows one example of the simulation using ML-PCM with a top heater. When the program current increases to 0.8 mA, the crystallization region expands to both side of the filament path.

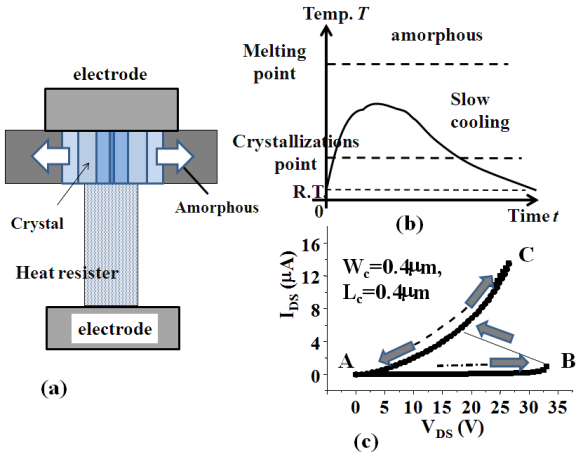

Fig. 2 Scheme of multilevel phase change mechanism, temperature control and I-V property in crystallization, (a) growth of crystal region, (b) temperature change and (c) I-V property.

2. 2 Increase of the resistance through amorphization using 2-steps pulse like a staircase

Figure 4 shows a scheme of ML-PCM changing the amorphous region by using controlling pulse shape. Figure 4(b) shows an ideal temperature control. The crystallization area increases with the temperature and the period. This means to need 2-steps pulse. We used the 2-step pulse, of which 1st pulse has a voltage of 11 V for 20 ns and 2nd pulse has 4 V for various pulse width of from 50 ns to 400 ns. Figure 5 shows the 2-steps pulse and the temperature rise up and down of the $Ge_2Sb_2Te_5$ (GST) in the device. A variation of maximum temperature of the PC material is shown in Fig. 6. The temperature is kept between crystallization point and melting point at ends of 2nd pulse. The amorphous area decreases with the 2nd pulse width so that we can increase the resistance to achieve the nonvolatile memory with random access.

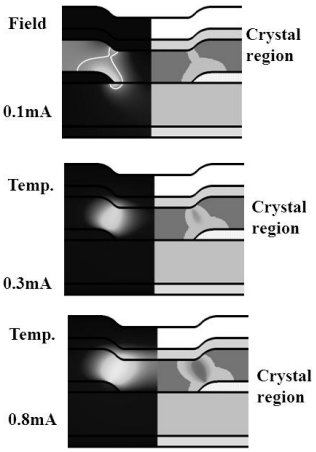

Fig. 3 Calculated field, temperature and crystal region at controlled currents of 0.1, 0.3 and 0.8 mA in amorphous region.

3. EXPERIMENTS&RESULTS

The ML-PCM structure was shown in Fig. 7. The top heater was used with TiSiN film with a resistibility of about $5.7x10^{-3}$ Ωcm and a thickness of about 80 nm. The resistibility was selected by requirement of minimum application voltage to obtain the critical field of about 38 V/μm for filament path and to directly heat the crystalline region without heating the heater for changing to amorphous state. Figure 8 shows optical images and SEM image of the prototyped ML-PCM with a top heater.

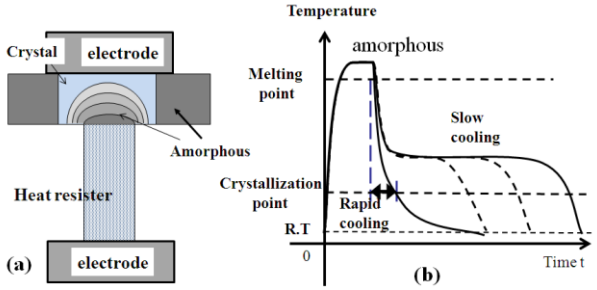

Fig. 4 Scheme of Temperature control for reducing crystalline region through amorphous and crystal phases.

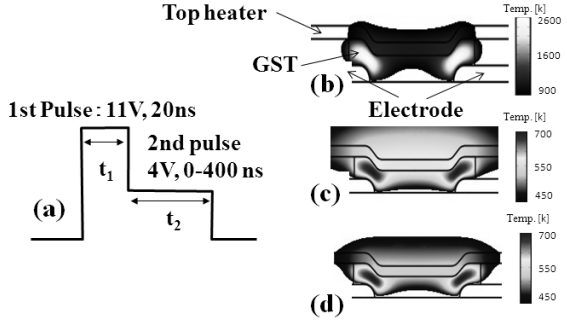

Fig. 5 Scheme of 2-steps pulse modulation and temperature rising distribution calculated by FEM method, (a) pulse form, (b) after 1st pulse application, (c) after 50 ns 2nd pulse application, and (d) after 100 ns 2nd pulse application.

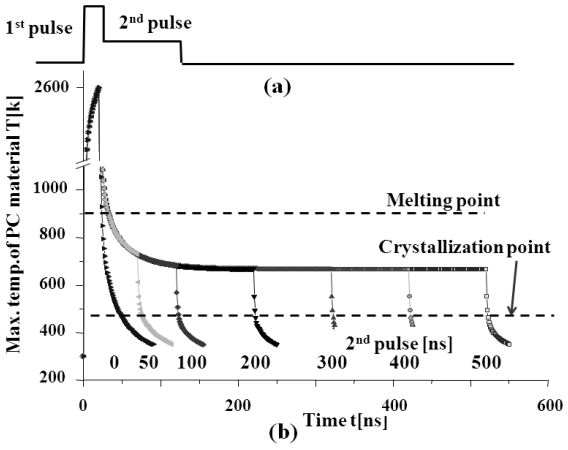

Fig. 6 Simulation results of maximum temperature of phase change material at applications of 2steps pulse like stair-case,(a) input pulse in a 2nd pulse width of 100 ns, and (b) maximum temperature at various 2nd pulse widths.

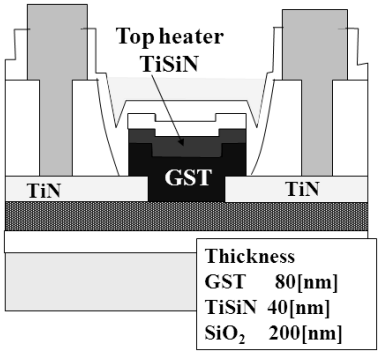

Fig. 7 Device structure of the prototyped lateral type phase change memory (L-PCM) with a top heater layer.

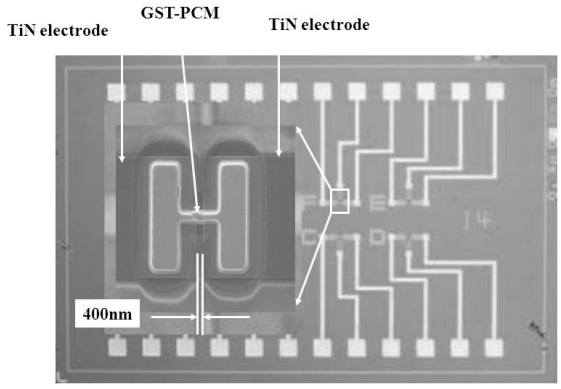

Fig. 8 Optical and SEM images of prototype device.

3.1 Decrease of the resistance from amorphous state

We obtained multi-level recording property to crystallize a part of the amorphous state as shown in Fig. 9. The PC material was SbTeN instead of GST. The heater was TiN with a resistibility of $2x10^{-3}$ Ωcm. The 1st step was from amorphous state to crystalline region at a program current of 0.4 mA. The resistance changed 27 kΩ in amorphous state to 12 kΩ in crystalline state. The 2nd step was done by applying the current to 0.8 mA. The resistance changed to about 8 kΩ. The result shows that the program current controls the crystalline region as the cross section is expanded in the amorphous region (Fig. 2).

Figure 10 shows another data that the resistances changed to various values from the amorphous state by the program currents of 30, 60 and 300 μA. The PC material and the top heater were GST and TiSiN materials, respectively. We could change the resistance from about 4 MΩ to about 30 kΩ by controlling the program current. The PC change is due to the cross section of crystalline region in the amorphous region.

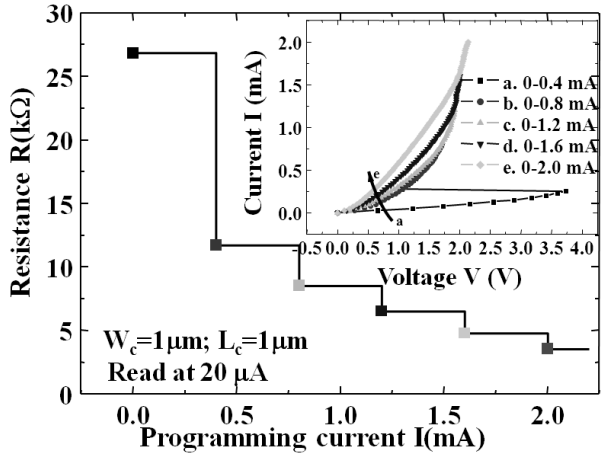

Fig. 9 Multi-levels recording using crystallization due to current control.

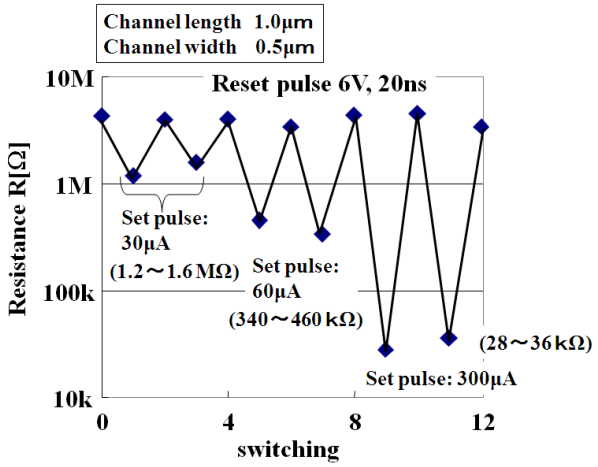

Fig. 10 Switching property using current control.

3.2 Increase of the resistance through amorphous state[5)]

When the 2-steps pulse was applied to the GST as shown in Fig. 5, we could increase the resistance from 40 kΩ to 500 kΩ as shown in Fig. 11. We could control the resistance by changing the 2nd pulse width of 400 ns to 50 ns as shown in Fig. 12. This means that crystalline region increases with the pulse width gradually after the PC material changed to amorphous region completely. The amorphous region decreases with the pulse width. The mechanism of phase change is due to changing the length of the amorphous region.

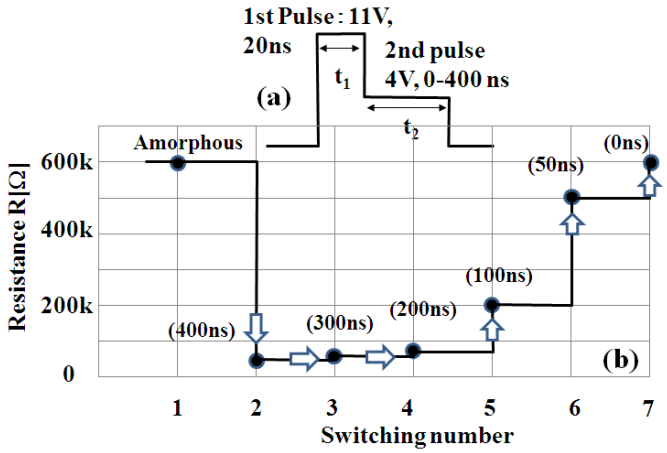

Fig. 11 Variation of the PC resistance by application of 2-steps pulse with various 2nd pulse width of 0 to 400 ns (the pulse width: ( )value).

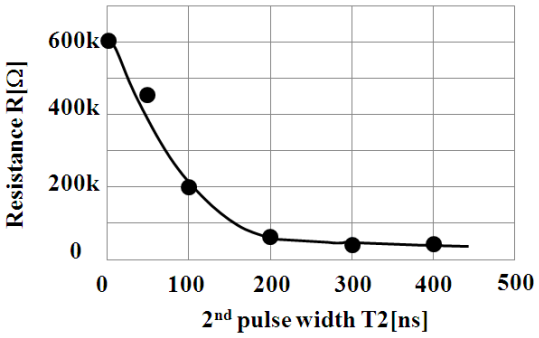

Fig. 12 Variation of PC resistance due to 2nd pulse width at applying a voltage of 11 V for 20 ns in 1st pulse.

4. CONCLUSION

We have studied the program current control and the pulse modulation for multi-levels lateral type (ML-) phase change memory (PCM). In order to use the ML-PCM as a random access memory (RAM), we have to develop a method to control the resistance from high to low or from low to high value for the memory access free. We have proposed ML-PCM using current control and 2-steps-pulse with various 2nd pulse width like a stair-case as one of pulse modulations for decreasing and increasing the resistance for the multi-levers recording, respectively. The simulation and experimental results have been obtained as follows.

(1) For decrease of the resistance from amorphous state, the program current can control the resistance to expand the crystallization region from shallow region such as the filament path.

(2) The crystallization region is made in amorphous region by current heating over the critical field.

(3) The resistance decreases due to the cross section of crystalline region made in the amorphous region.

(4) For increase of the resistance through amorphous state, the 2-steps pulse and its 2nd pulse width can achieve the increase.

(5) The 2nd pulse width can control the amorphous region to reduce the amorphous region from complete amorphous region.
(6) The resistance increase is due to changing the length of the amorphous region.

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Biographies

Sumio hosaka was born in Japan in 1948. He received the Ph. D. degree in Engineering from Waseda University, Tokyo, in 1983.

He joined the Hitachi Central Research Lab. (HCRL), Co. Ltd. Kobunji, Tokyo in 1971, working in semiconductor lithography using electron, ion and light beams, nano-metrology using electron beam and scanning probe microscope (SPM) techniques, in HCRL and terabyte huge storage using SPM in the Hitachi Advanced Research Lab. (HARL). After he joined the Hitachi Kenki Finetech Co., Tsuchiura, Ibaraki in 1999, working in-line atomic force microscope products, he joined Department of electronic engineering, Gunma University, Kiryu, Gunma, in 2000. Since 2000, He has been professor in the university, and is working on nano devices such as QCAS and phase change memory, nano fabrication such as EB writing and self-assemble nano dot arrays, and nano metrology based on SPM.