# Progress of Phase Change Non Volatile Memory Devices

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*(invited paper)*

## ABSTRACT

Phase-change memories (PCM) are resistive memory devices which are emerging as the only promising alternative to the mainstream Flash technology. Recent results have demonstrated good scalability perspectives, fast write/erase speed and exceptionally long endurance. Despite the industrial results demonstrating the technology potentials, the device physics is still under investigation. In principle, PCM operation is simple. It relies on phase change transition of a thin-film chalcogenide layer, which makes the cell resistance change between two bit values. However a quantitative description of the cell operation is highly challenging. Carrier transport phenomena (high-field multiplication, recombination, threshold switching) are coupled to thermal induced phase change (melting, glass transition and crystallization through nucleation and growth), while transient phenomena affect the solid amorphous structure of the chalcogenide layer causing a drift of the memory resistance. The paper reviews the physics underlying PCM cell operation, the chalcogenide band-structure model used in numerical simulations of the device operation, the description adopted for the amorphous/crystalline phase transition as well as the evidence of transient effects like threshold/resistance recovery and drift. Finally a unified key figure of merit to compare the different cell architectures is proposed.

**Key words**: phase change memories, chalcogenide materials, non-volatile memories.

## 1. INTRODUCTION

Starting from their introduction in the late 80's Flash memories have become the mainstream non volatile memory technology. The market size of these devices has rapidly increased and in the last decade these devices have been the key drivers of the booming digital consumer market. The NOR Flash, adopted for code storage, features a cell size of $10\text{-}12F^2$, where F is the technology feature size (Figure 1). The NAND Flash products, optimized for sequential data storage, have been scaled more aggressively reaching a cell size of about $4.5F^2$. However, as the 45nm technology node is approaching, fundamental issues are setting clear roadblocks to further scaling. As the scaling proceeds all the linear dimensions have to be shrunk, including also the thickness of the dielectric layers which avoids charge losses from the floating gate. The thinner the insulating layer, the worse data retention. On the other side, the smaller the device area, the smaller the number of electrons stored, the smaller the acceptable charge loss. At the 32nm node, the maximum acceptable leakage from the floating gate should be less than 10 electrons over ten years. As the conflict between insulator scaling and data retention is becoming potentially unsolvable, other memory concepts are therefore being explored to find alternative non-volatile devices at the nanoscale.

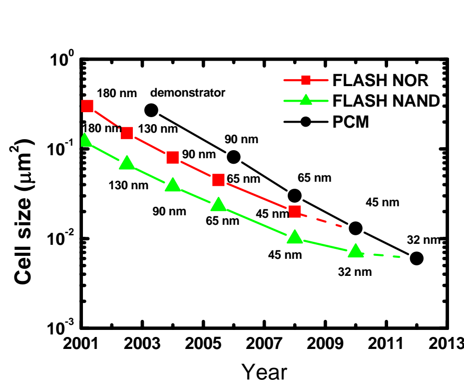


**Figure 1** – Scaling trends for NAND, NOR and PCM. The phase change memory technology is expected to reach the same Flash-NAND size at the 32 technology feature size.

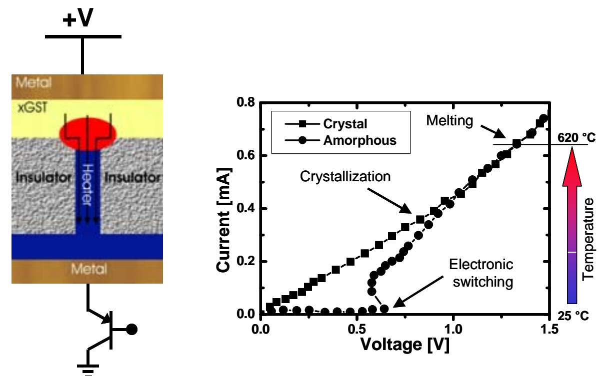


**Figure 2** – PCM cell is constituted by one tuneable resistor (the storage element), and by one transistor (the selecting element). Depending on the phase of the GST, the device features the electrical behaviour in the left.

The principle of a chalcogenide RAM memory was proposed in 1962 [1], however, only in the early 2000's, the semiconductor industries have started to consider Phase Change Memories (PCMs) a promising candidate to eventually become the next mainstream non-volatile technology. In 2001 Intel-Ovonyx presented the first industrial memory array using PCM memory cells[2], then followed by demonstrators from STMicroelectronics [3] and Samsung [4]. Due to the fast program and access times, the large cycling endurance [5, 6] and the extended scalability [7, 8] this technology is considered the only real option for the post-Flash scenario. Figure 1 shows a roadmap of PCMs evolution compared to the Flash benchmark. Starting form the first industrial demonstrators at the 180nm technology node, the PCM cell size (8-10$F^2$) is expected to reach the NAND cell size around the 32-nm node and has the potential to be further scaled without meeting major roadblocks down to the 16nm technology node. Moreover the memory is ideally suited to store more than two levels per cell, thus giving an additional option to further reduce the cost per bit.

## 2. CELL OPERATION AND PERFORMANCE

The PCM memory cell is characterized by one transistor, used as bit selector, and one resistor (Figure 2). The active layer is the chalcogenide layer ($Ge_2Sb_2Te_5$, or GST) sandwiched between a top metal contact and a resistive bottom electrode (the heater). Depending on whether the chalcogenide material is crystalline (*set* state) or amorphous (*reset* state) the cell resistance changes by orders of magnitudes. Figure 2 also shows the I-V curves of the cell in the *set* and *reset* states. In the *reset* state the cell is highly resistive (in the MΩ range) at low bias. As the voltage rises above a threshold value, $V_{TH}$, the voltage snaps-back and the cell becomes conductive. The I-V curve of the SET does not feature any threshold. The slope of the curve is mainly determined by the heater resistance.
Memory programming relies on joule heating. In the *set-reset* transition, the cell, initially fully crystalline, is driven by a 50-100ns current pulse. Joule heating makes the temperature of the chalcogenide layer close to the bottom electrode (heater) rise above the melting temperature ($T_M$=620°C). The molten material is then swiftly cooled down following the nanosecond trailing edge of the current pulse. The transition leaves an amorphous GST region capping the heater. For the opposite transition, the cell is driven by a similar current pulse but with a lower peak value. The pulse heats up the GST close to the bottom electrode around 550°C. This temperature is lower than $T_M$ but it is high enough to make the spontaneous amorphous-crystalline transition happen in about 100ns. The memory can therefore switch between two resistive states using fast, nanosecond current pulses.
Reading is accomplished by biasing the cell at 0.1-0.2V and sensing the current. The 50-100μA current flowing through a cell in the *set* state is able to load the bit-line capacitances of a memory array in less than 50 ns. The current through a cell in the *reset* state is instead not able to trigger the sensing amplifier, leading to the evaluation of a "0". Moreover, PCM cells show excellent reliability. The two states retain a resistance ratio larger than $10^2$ over $10^{11}$ programming cycles, a cycling endurance much larger than Flash products.
However, the most critical issue for a nonvolatile memory is data retention The *reset* state of the PCM is particularly critical, since amorphous GST can spontaneously evolve towards the most stable crystalline phase. Figure 3 shows the Arrhenius plot for the failure time, defined as the time required to the resistance of a cell in the *reset* state to decay to a resistance value equal to the geometrical average between set and reset resistances. The experimental activation

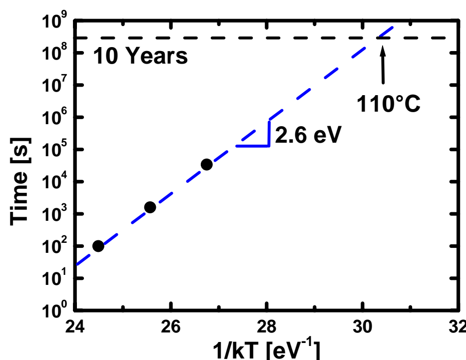


**Figure 3 -** Experimental crystallization time of the reset state as a function of temperature in the Arrhenius plot. A maximum temperature of 110°C can be tolerated to guarantee 10 years data retention.

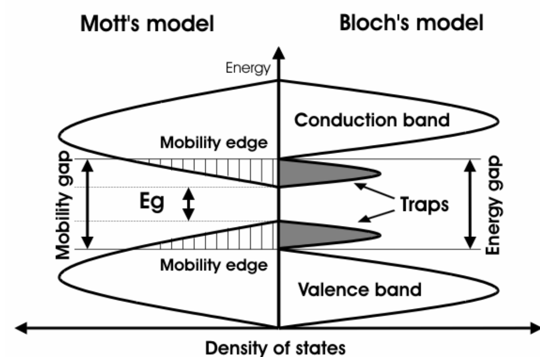


**Figure 4** – Comparison between the classical Mott and Davis's picture for the amorphous band diagram and the one recently proposed by Pirovano et al. [12].

energy of 2.6eV corresponds to 10-years lifetime at the maximum temperature of 110°C. These data have been also verified on a statistical basis, confirming that 10 years data retention at 85°C can be easily granted for a bit distribution.

## 3. MATERIAL PROPERTIES AND TRANSPORT PARAMETERS

The properties of chalcogenide glasses began to be investigated in the late 1960s [9], when some attempts were made to understand the electrical memory effect in different amorphous compounds. Nowadays it is clear that the crystalline GST has two possible structures: a stable hexagonal structure and a meta-stable face centered cubic (FCC) lattice [10]. Since the metastable phase crystallizes faster [11], in PCM operation the crystalline GST is probably in the FCC phase. In this structure all atoms have a six-fold coordination, with a sublattice randomly occupied by Ge and Sb and the other by Te atoms [11, 12]. Due to the stoichiometry, 20% of the Ge–Sb atomic sites are indeed vacant [13], [14] making the crystalline GST regarded as a p-type semiconductor with a 0.5eV gap [15].
The microscopic structure of amorphous GST is still under investigation. Carrier transport in this material is limited by a large density of localized states with low mobility [16, 17, 18]. In the ’60 it became a common practice to describe these materials as in Figure 4-left [19, 20], where “mobility edges” separate fully conductive bands from low mobility states. However, by assuming that low mobility localized states behave like trapping centers and that more conductive levels resemble delocalized states, amorphous GST can be depicted as a “very defective” crystalline semiconductor [12] with the band structure model reported in Figure 4-right. The low mobility states are replaced by a high density of traps close to the band-edges.
In Table I such levels are denoted as C-type, following the idea, largely agreed in literature, that most of these traps may be due to a donor-like level ($C_3^+$) close to the conduction band, generated by three-fold coordinated chalcogen (Tellurium) atoms. An acceptor-like level ($C_1^-$) is instead placed close to the valence band-edge, due to one-fold coordinated Tellurium atoms. The adoption of a semiconductor-like model for both phases is a key step enabling the use of a numerical device simulator for the study and optimization of PCM cells.
The transport properties of the GST layer has to be completed introducing a carrier generation mechanism. This step is suggested by Figure 5. Note that before threshold switching the current starts to rise exponentially suggesting the presence of carrier generation in the amorphous cell due to tunnelling or impact ionization. However differently from tunnelling, only impact ionization gives rise to a multiplication rate dependent on current and, as highlighted first by Adler [21], such a dependence is essential to account for switching.
Figures 6 shows the band-diagram as computed by the device simulator along the cross section in the middle of the PCM cell. Note the amorphous GST layer with the wider band-gap, while the heater has been modelled as a heavily p-doped semiconductor, featuring an Ohmic contact with the GST. At low bias the quasi Fermi levels are close to the equilibrium position (Figure 6 on Top). As the bias rises, impact ionization takes place at the cathode side while the defects close to the anode become pathways for carrier recombination. As these traps become fully occupied, the

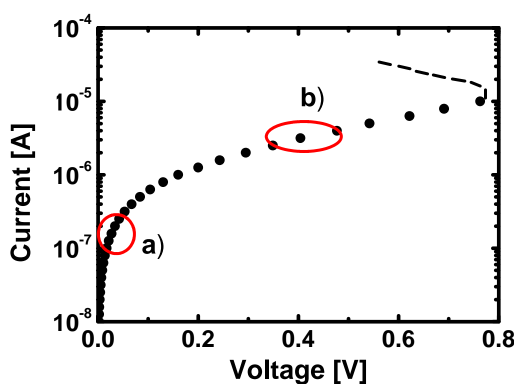


**Figure 5 -** Experimental low field electrical characteristic for the amorphous GST. Two different region can be found: a) Ohmic behaviour, b) exponential increase of the current with applied voltage.

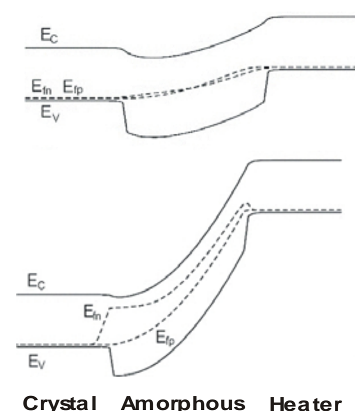


**Figure 6** - Band diagrams corresponding to the working points a) and b) of Fig. 5. For low field applied quasiFermi levels are closed to the equilibrium value. Increasing applied voltage, the generation properly balances the recombination thought trap levels. When recombination saturates, generation finds a new stable working point reducing the voltage across the device.

| Property | GST crystalline | GST amorphous |
|---|---|---|
| $E_{gap}$ [eV] | 0.5 | 0.7 |
| $N_c$ [cm$^{-3}$] | $2.5 \times 10^{19}$ | $2.5 \times 10^{19}$ |
| $N_v$ [cm$^{-3}$] | $2.5 \times 10^{19}$ | $10^{20}$ |
| Vacancies [cm$^{-3}$] | $5 \times 10^{20}$ | - |
| $C_3^+$ [cm$^{-3}$] | - | $10^{17} \div 10^{20}$ |
| $C_1^-$ [cm$^{-3}$] | - | $10^{17} \div 10^{20}$ |
| $\mu_n$- $\mu_p$ [cm$^2V^{-1}s^{-1}$] | 0.1–23.5 | 5–200 |
| $F_C$ [$Vcm^{-1}$] | $3 \times 10^5$ | $3 \times 10^5$ |

**Table I** – Electronic parameters for both crystal and amorphous phases.

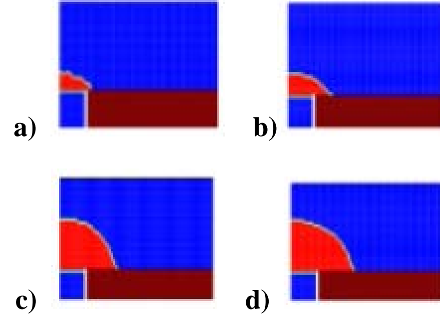


**Figure 7** – Amorphous regions at the end of a programming pulse obtained by increasing the peak current value. A bigger amorphous region corresponds to higher resistance level.

electron Fermi level close to the anode approaches the conduction band-edge denoting that the free electron density near to the anode is rising, lowering the material resistivity. Such a resistivity drop causes an increase of the current injected from the anode which, in turn, makes the carrier generation rate at the cathode rise further. The system is therefore positively feedback.

As the loop gain becomes larger than one, threshold switching takes place. A snap back of the voltage quenches the generation rate [12], while the large amount of free carriers sustain the generation rate at the cathode even if the multiplication rate has been drastically reduced. In conclusion, for threshold switching to occur the dominant generation rate must be dependent not only on the electric field but also on carrier density. Impact ionization is the most natural candidate. The avalanche multiplication has been described using the Okuto-Crowell model [22] with a critical field of $3x10^5$ cm for both holes and electrons.

## 4. PHASE CHANGE DYNAMICS

Since PCM memory relies on the phase transitions, a detailed understanding of the phase-change mechanisms is essential to develop optimized memory cells. To this purpose, numerical simulations of the PCM dynamics have proven to be a valuable tool to bridge the experimental results and the microscopic structure of amorphous and crystalline phases in the active volume of the cell. These studies have been performed using a semiconductor device simulator coupling the material and transport model described in the previous section to the heat conduction equation to describe self-heating (Joule effect) together with the GST nucleation/crystallization dynamics[23].

Let us first consider the *set-reset* transition. In this case the cell start from the crystalline state and, due to Joule heating, the GST is molten. Figure 7 shows the thickness of the amorphous layer left at the GST-heater interface after a 50ns programming pulse as the peak programming current rises from 450μA to 800μA. The hot spot and the

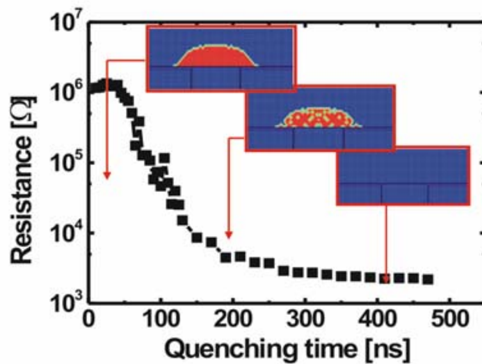


**Figure 8** – Resistance obtained by increasing the falling time of the programming pulse. For longer quenching time, crystallization takes place and a lower resistance level has been achieved.

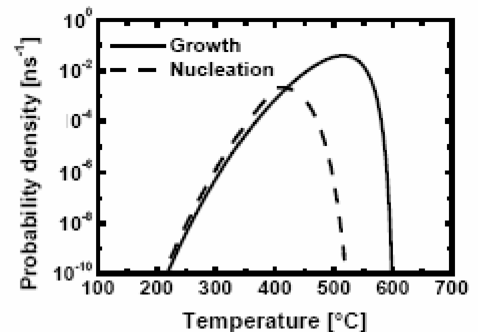


**Figure 9** – Nucleation and growth probabilities as a function of temperature. Nucleation randomly occurs crystallizing an amount of amorphous equal to the critical cluster volume while growth proceeds from pre-existing crystal interfaces.

amorphous zone gets wider, still maintaining a hemispherical shape. The thicker the amorphous layer, the higher the resistance value of the cell left in the *reset* state.
The trailing edge transition of the current pulse is of key importance. If the current is switched off in a very short time (10-15 ns) crystallization does not have time to occur while the GST is cooling down. If the quenching time lasts more than 100ns, crystallization starts and small nuclei appear in the amorphous GST leading to a lower final cell resistance (Figure 8). During the numerical simulation, nucleation has been introduced using a Monte Carlo approach, by sorting at each time step the probability for an elementary amorphous volume, about 2.2 $nm^3$ large, to become crystalline.
A similar framework can be adopted to include crystalline growth [24, 25]. In this latter case the only care is to sort for phase transition only among elementary volumes already adjacent to crystalline tiles. Figure 9 shows the dependence of the nucleation and growth rates as derived by calibrating the parameters against experimental results. While the nucleation rate does not depend on the volume size, the growth rate has been quoted taking the inverse of the time needed for the crystal/amorphous interface to move by the numerical grid size ($L_g$= 1.2 nm). In this way the units are the same and the values can be reported on the same scale but the growth probability depends on grid size.
The bell shape dependencies can be explained in the framework of the classical nucleation/growth theory. The steady state nucleation rate can be written as:

$$I \propto h \exp\left(-\frac{E_a + \Delta G_C}{kT}\right)$$

where $h$ contains a negligible temperature dependence, $E_a$ is the activation energy for atomic mobility and $\Delta G_C$ is the free energy required to form a nucleus of critical radius [24]. The rise of the nucleation rate in 100-350°C temperature range follows the Arrhenius improvement of the atomic mobility in the amorphous matrix. The drop at higher temperature is instead due to the steep increase of the critical nucleus size and of the corresponding free energy barrier $\Delta G_C$ as the temperature approaches the melting temperature. The growth rate dependence is similar. The growth rate increases as the atomic mobility rises, while the drop is related to the decrease of the free energy gain of the phase change approaching the transition temperature [26, 27].
From a quantitative standpoint the growth rate drops at higher temperature with respect to the nucleation. It follows that for temperature lower than about 400 $^oC$ nucleation and growth occurs together, while for higher temperature growth is favored with respect to nucleation. Note that the classical nucleation/growth theory applies at steady-state and under isothermal conditions while none of these conditions are fulfilled during the programming transients of a PCM cell. The values in Figure 9 should therefore be regarded as effective values and it would be highly challenging to quantitatively account for them.
Figure 10 shows simulation of the nucleation and growth dynamics in the *reset-set* programming pulse. Note that the current fires first along a narrow filament starting from the edge of the heater/GST interface. This is due to the electronic switching. Since the effect is highly sensitive to the local electric field, switching takes place along the path where the electric is maximum. The simulation highlights that current remains highly localized as well as the Joule heating. Nucleation and growth follows the same path and if the current pulse is short, only a narrow crystalline road has been open through the amorphous dome. The resistance of the cell after such a programming pulse is still large.

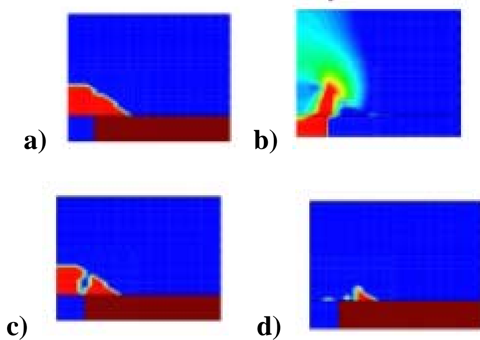


**Figure 10** – Programming operation from amorphous to crystal state. Because of the electronic switching, current first spikes where the amorphous thickness is minimum, locally increasing the temperature. Nucleation and growth, then, occur extending the transformed volume.

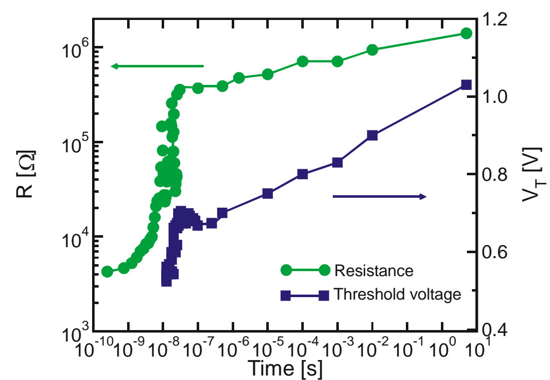


**Figure 11** – Low field resistance and threshold voltage for the amorphous phase as a function of time after reset programming operation. In about 50 ns both low field resistance and threshold voltage are recovered, then they still increase due to the drift phenomenon.

Only increasing the duration of the current pulse or by using a larger peak current value, the entire amorphous layer has time to switch back to the crystalline phase, thus recovering the minimum resistance value for the *set* state.
Figures 7 and 10 suggest that by changing the programming pulse, the value of the cell resistance can be reliably placed in between the largest and the minimum SET value. These options open the way to a multi-bit operation. For example four levels, with different resistance values, might be programmed per cell, thus reducing the cost per bit. However, some transient effects might impair such an opportunity.
$V_{TH}$ and R are two key parameters of the memory cell. Figure 11 shows the time dependence of these parameters as measured soon after the current pulse programming the cell in the *reset* state. The first fast component of the transient is referred to as recovery. On the longer time scale, in the so-called drift regime, the $V_{TH}$ and R transients follow a slower power law. As far as memory operation is concerned, the recovery sets the minimum time needed after programming before reading. If the cell is read soon after being programmed in the *reset* state, the read value might erroneously be “1”. Drift of the amorphous GST is not instead an issue for single bit memory cells. The resistance difference between the two states increases, thus making larger the noise margin during the readout. Drift is instead a limit for multi-bit operation since the resistance of an intermediate level during ten years ($3x10^8$ sec) might cause the bit to be erroneously decoded.
Different models have been proposed to justify these effects. Recovery is likely due to charge transients. After quenching, the newly formed amorphous region is full of trapped carriers. Some nanoseconds are needed for these carriers to be released by trapping states and for the Fermi levels to recover the equilibrium value (Figure 6a). During this transient $V_{TH}$ and R changes from the *set* to the corresponding *reset* values.
Drift physics is instead more controversial. It has been suggested that drift might be due to mechanical stress release following the crystalline-to-amorphous phase transition. The resulting band-gap widening may reduce the mobile carrier density contributing to charge conduction. Another possible explanation links the effect to changes of the electronic states [28] (variation of the density of states close to the band-edge) already observed in other chalcogenide compounds [29] as the amorphous evolves towards to a more regular microscopic structure. For multi-bit storage to be implemented in PCM memories this effect should be fully understood and minimized.

## 5. FIGURE OF MERIT OF PCM CELLS

Literature results are encouraging. From the first industrial results on PCM cells, presented by Intel-Ovonyx [2], several solutions, involving different cell architectures [3, 30, 31] and the adoption of N-doped or oxided GST [32, 33], have been proposed. The main goal being the reduction of the programming current. Figure 12 summarize the programming current values reported in the last three years as well as the scaling trend as a function of the bottom contact area. However, the bottom contact area is not the only parameter entering the overall electro-thermal design of the cell. Even using the same bottom contact area, different cell architectures, with different size/doping of the active GST layer and bottom contact size, feature different programming currents and resistance values. Moreover, record low programming currents are often claimed but at the expenses of a large cell resistance in the *set* state. In fact there is a trade off between the two figures. A low programming current can be reached by tightly confining the current flow and the corresponding heat generation. This usually results in a high cell resistance.
Note that there is an upper limit to the acceptable *set* resistance value. The lower the cell current during the read operation, the longer the time needed to charge the bit-line capacitance. In practice, for a read operation to happen

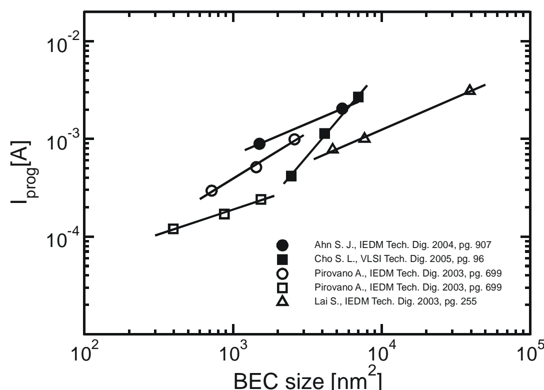


**Figure 12** – Programming current as a function of bottom contact size from different published works. The data are related to several cell architectures.

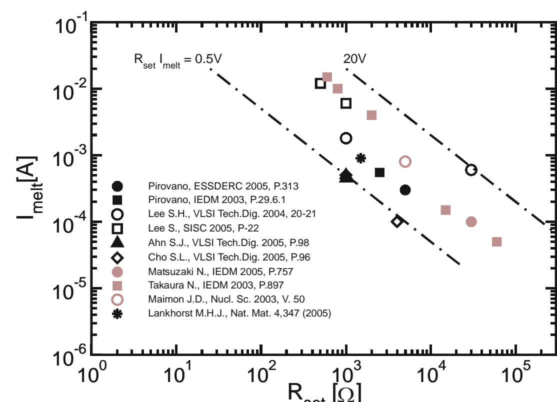


**Figure 13** – Melting current vs. set resistance for devices from literature. The Imelt-Rset product is a key figure of merit of PCM technology.

within 50ns the *set* resistance should be kept lower than 50kOhm. It is therefore more meaningful, from the application standpoint, to compare the different results by quoting the product $R_{set}$ $I_{melt}$, where $I_{melt}$ is the melting current defined as the current needed to obtain twice the set resistance (Figure 13). The constant $R_{set}$ $I_{melt}$ lines are highlighted by the dashed lines. The figure clearly shows the potential for these cells to reach programming currents of few tens of μA.

## 6. CONCLUSIONS

Phase change technology has made great progress in last decades. The paper has reviewed the current understanding of PCM operation, the models adopted to perform device simulations and to optimize cell performance. Simulation results of phase-change dynamics have been presented and the corresponding microscopic mixture of amorphous/crystalline phases has been discussed. The potential of multi-bit operation has been highlighted together with the impact of transient effects. Finally the experimental results obtained with different cell architectures have been reviewed and compared based on a unified key figure of merit.

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**Biographyies**

Born in 1962. In 1985 he received the Laurea degree in Nuclear Engineering from the Politecnico di Milano, Italy. From 1987 to 1992 he was member of the research staff of the Italian National Research Council. In 1989-90, he was Visiting Scientist at the AT&T Bell Laboratories, Murray Hill, NJ. In 1992, he was appointed Associate Professor of Electronics at the Politecnico of Milano and since then, he has been teaching courses on electronics, electron devices, analog electron design, optoelectronics and solid-state physics. In 1993 he established the Microelectronics Lab. In 1999, he has been Academic Visitor at IBM T.J. Watson Research Center, Yorktown Heights, NY. In 2000, he was appointed Full Professor of Electronics at the Politecnico di Milano.
As researcher, he has contributed in many fields from optoelectronics to electronic instrumentation design, from integrated analog circuit design to microelectronic device physics. In microelectronics he has contributed to device physics pointing out the limitations set by quantum effect in ultra-scaled MOS transistors, studying the technology and reliability of non-volatile Flash memories and, more recently, pioneering the development of chalchogenide Phase Change Memories. He is co-author of more than 200 papers published in journals and presented in international conferences. He has now serving as Chair of the Department of Electronics and Information Technologies at Politecnico di Milano.