

New metrics for chalcogenide material optimization in PCMs

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ABSTRACT

A new methodology for thermal properties extraction is presented and applied to different cell geometries and different chalcogenide alloys. The new method allows the extraction of the material melting temperature and the cell thermal resistance which are useful parameters for material optimization. The methodology has been also applied to scaled devices allowing the assessment of proper scaling rules for the thermal parameters. The cell reliability and performance are then discussed and compared on a set of tellurium-poor GST alloys. The set current and the cell retention capabilities are compared as a function of stoichiometry, showing that a proper material engineering can straightforwardly modulate the cell performances and reliability according to the application requirements.

Key words: Phase change memory, chalcogenide alloys, reliability, melting temperature, crystallization, thermal resistance.

1. INTRODUCTION

The phase change memory devices have reached a production maturity level with available products at 90 and 45 nm nodes. Despite technology being developed with very good results both from the performance and the reliability points of view, some physical parameters of the chalcogenide material governing the cell functionality are difficult to be measured when integrated in nano-scaled devices. Material optimization is not thus straightforward and often the methodology for cell optimization follows an experimental approach instead of theoretical guidelines. In particular the thermal parameters are difficult to be measured during the memory operation when high current density and high temperature gradient are present within the device. In the first part of this work a new methodology for thermal properties extraction is shown and applied to different cell geometries and different chalcogenide alloys. The new method allows the extraction of the melting temperature and the cell overall thermal resistance, useful for material optimization. The methodology has been also applied to scaled devices allowing the assessment of proper scaling rules for the thermal parameters. A set of tellurium-poor GST alloys are then compared in terms of the cell performance and reliability. Programming window and retention are compared as a function of stoichiometry, showing that material engineering is a possible path toward the direction of properly tuning the cell performances and reliability in view of the particular application.

2. EXPERIMENTAL METHODOLOGY

A method for physical material parameter extraction such as the melting temperature and the thermal resistance on integrated devices is described in this section. The method is based on electrical measurements relying on the study of the resistance–power (R - P) curves taken on Ge-Sb-Te (in the following GST) based Phase Change Memory cells (PCM) in the 90-nm technology node [1], as shown in Fig 1. The power associated to each measured R point is obtained by combining the measurement of the R - I and I - V pulsed characteristic curves, according to the relation $P = VI$. The R - P data in Fig. 1 are obtained at different external temperatures T_{ext} .

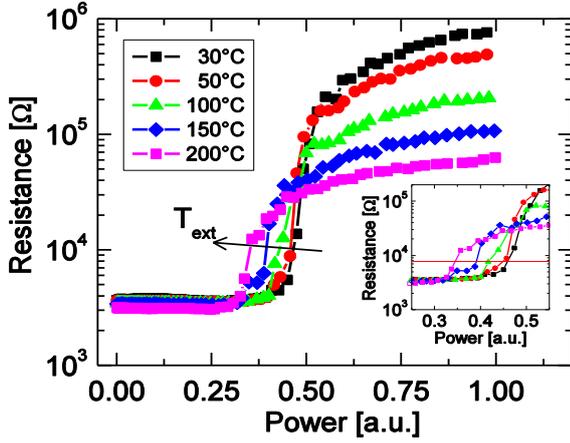


Fig.1: Programmed resistance versus programming power for different environment temperatures. In the inset: a clear shift in the melting power is expected for different external temperatures.

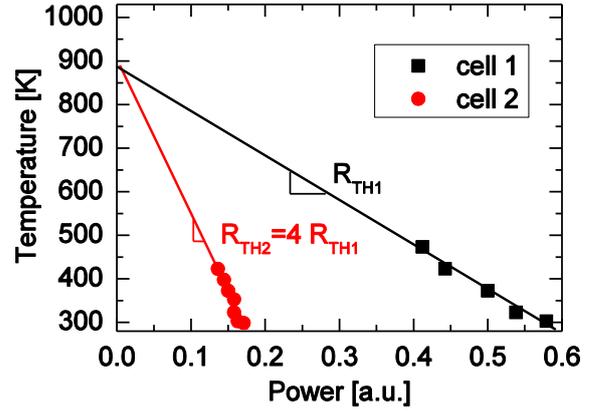


Fig. 2: External temperature vs programming power extracted from the data in Fig. 1. The slope of the curve is the thermal resistance while the intercept is the melting current. Cell 2 is a miniaturized version of cell1, applying a scaling factor of 4.

namely, 25, 50, 100, 150, 200 °C, forced by a thermo-chuck on which samples are fixed. Different external temperatures result in two different effects on the R - P curves. On one hand an increasing T_{ext} results in a decreasing amorphous/crystal resistance, according to the conduction activation, namely, $E_C=0.02$ eV for crystalline set state and $E_C=0.3$ eV for the amorphous full reset state.

On the other hand, Fig. 1 highlights a shift of the set to reset edge of the program curves to lower power for increasing external temperature. Indeed, the higher the external temperature, the lower the power injection required for the electrically driven melting of GST [2]. Inset of Fig. 1 focuses on the set to reset edges as a function of T_{ext} , showing the edge shift. By integrating the heat transport equation, a simple relationship between the injected power, P_{prog} , and the internal temperature during the program operation, T_{prog} , can be achieved:

$$T_{prog} = T_{ext} + R_{th} \cdot P_{prog}, \quad (1)$$

where T_{ext} is the external temperature forced by the thermo-chuck, and R_{th} is the overall thermal resistance. Consider now a particular device status, *e.g.*, the material melting condition, defined as the formation of an amorphous thin film on the heater–GST interface and production of the very first R increase from the set state. In this case, the equation can be simply written as

$$T_{melt} = T_{ext} + R_{th} \cdot P_{melt}. \quad (2)$$

T_{melt} is thus reached owing to the superposition of the forced T_{ext} and the electrical power injection contributions through the Joule effect. Since the melting temperature and the thermal resistance are material parameters and they are not expected to depend on the external temperature, it is possible to differentiate equation (2) easily finding the condition that

$$R_{th} = - \frac{dT_{ext}}{dP_{melt}}. \quad (3)$$

R_{th} can be thus easily extracted by performing different experiments conducted at different external temperatures and measuring the required electrical power to get the melting condition of the GST. By substituting eq. (3) into eq. (2), the melting temperature can be also extracted. Fig. 2 reports the relationship between the external temperature and the melting power for two different cells with different geometry but realized with the same

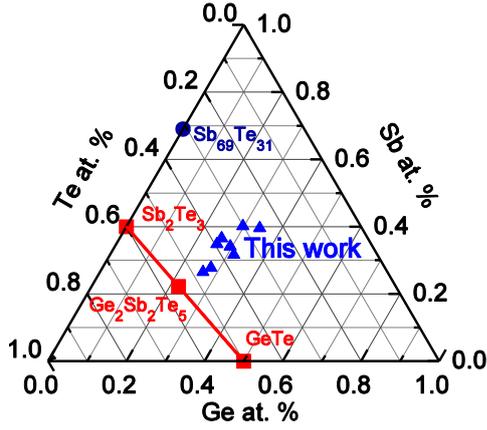


Fig. 3: GeSbTe compositions explored in this work, starting from $\text{Ge}_2\text{Sb}_2\text{Te}_5$ toward the Te-poor direction.

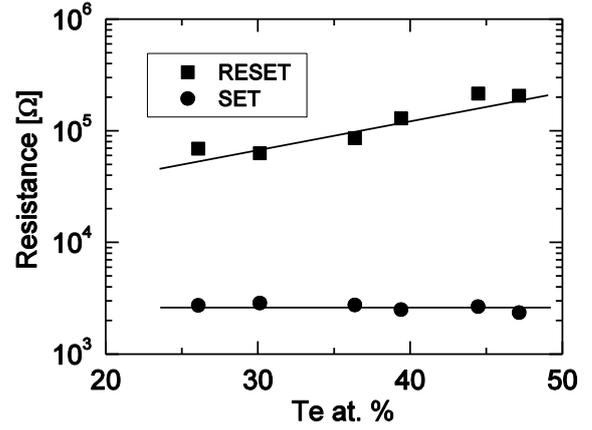


Fig. 4: Resistance window as a function of Te content for the GST alloys explored in this work. A clear dependence from Tellurium content is shown.

chalcogenide active material ($\text{Ge}_2\text{Sb}_2\text{Te}_5$). As expected the extracted melting temperature is the same while the thermal resistance changes according to the geometry of the cell.

The two measured cells are realized with the same cell architecture (the wall architecture reported in [1]), but at different lithographic nodes. As expected, the scaled device has a higher thermal resistance as a result of the cell shrink, while the melting temperature of the chalcogenide material is not scaling-dependent. The method allows an electrical-based melting temperature estimation and the extracted value is very close to those expected from the literature [3], namely, $T_{melt} > 880$ K. The different slopes of the T - P diagrams taken for the two cells account for the aggressive scaling factor applied between them: the thermal resistance R_{th} increase of a factor 4 is consistent with the shrink of the device by the same factor, providing a linear scaling rule for this parameter. Finally, it is worth noting that also the electrical power required to get the melting condition decreases with the device downsizing from 0.6 to 0.15 (at room temperature), consistently with the PCM scaling rules.

3. RESULTS & DISCUSSION

In this section, we focused on some alloys toward the Te-poor direction in the GeSbTe ternary diagram, away from the widely studied $\text{Ge}_2\text{Sb}_2\text{Te}_5$, or the standard GST, lying on the pseudo-binary line between GeTe and Sb_2Te_3 as represented by the blue points in Fig. 3. The main parameters we monitored are the resistance window, data retention and power consumption during the phase change operation.

A sufficient resistance window between the two phases of GST is required to have a good readout margin for device operation. Figure 4 reports the set and reset resistance behavior as a function of the Te relative concentration. Increasing Te allows a more resistive reset state (amorphous GST), widening the resistance window and enhancing the readout margin. Figure 5 reports the behavior of the current required to reset the cell, I_{RESET} , and the current to set the cell, I_{SET} , as a function of Te content, both increasing toward the Te-poor direction. Since a decreasing melting temperature from 870K to about 800K, is expected decreasing the tellurium content from literature [4, 5] and reported in Fig. 7, the result on the reset side is somehow unexpected. Such behavior was attributed to a possible variation of the thermal conductivity of GST as a function of composition analyzed in the following.

For a more complete characterization of the GST compounds, reliability in terms of data retention has been also evaluated. To this purpose we consider a metrics able to highlight the lattice / network topology of a GST compound [6]. It is based on the calculation of the average coordination number of a ternary GeSbTe alloy as:

$$r = 4X_{Ge} + 3X_{Sb} + 2X_{Te}, \quad (4)$$

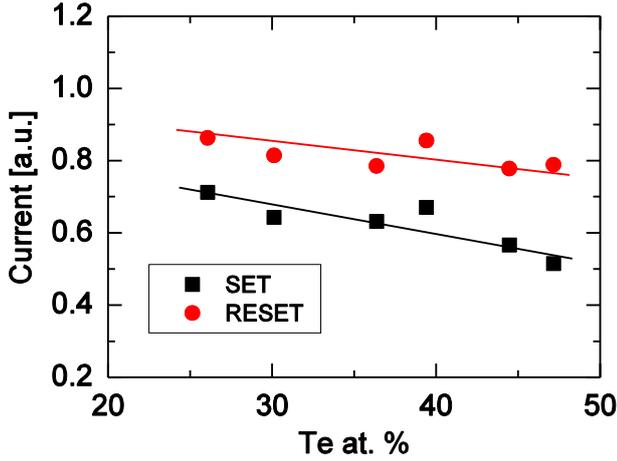


Fig. 5: Programming parameters for GST compounds explored in this work as a function of Te content. Programming currents decrease by increasing the tellurium content in the alloy.

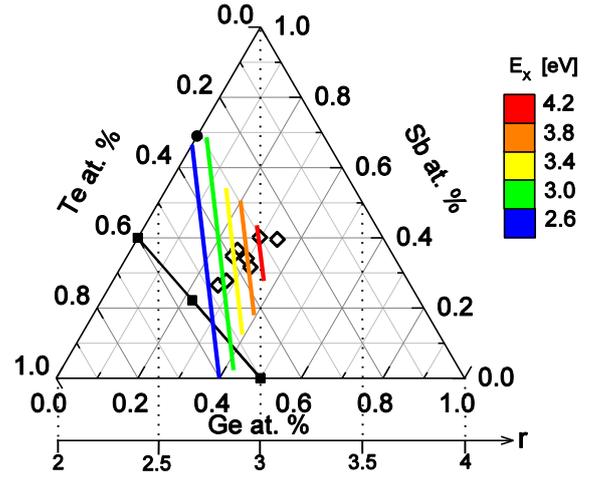


Fig. 6: Retention performance of the different studied GST composition. The higher the average coordination number, the higher the activation energy.

in which X_Y represents the relative concentration of the Ge, Sb and Te elements; 4, 3 and 2 represent the valence numbers of Ge, Sb and Te respectively. Thus r denotes the number of nearest neighbors each atom has within the disordered network on the average. The higher r the higher is the average network connectivity and/or structural rigidity of the alloy. Hence moving toward Te-poor compositions allows ruling higher values of r , namely allows for an over-coordinated network, thanks to the increased weight of the valence numbers of Ge and Sb on the overall r with respect to the Te one. Higher connectivity alloys are expected to show on one hand improved retention capabilities of the amorphous phase and on the other hand an increasing current for the set operation at fixed time due to an over-linked structure to be annealed during the reset to set transition. Both expected trends are confirmed. Fig. 6 reports the crystallization iso-activation lines: apparently the crystallization activation energy E_X increases toward the Te-poor direction. E_X has been extracted by computing the Arrhenius law of the crystallization characteristic times obtained thanks to isothermal measurements of the reset resistance with time [7]. Fig. 5 then shows an increasing fashion of the set current I_{SET} toward the same composition direction, in a 300 ns width set pulse condition. Both results are interpreted in the framework of the average coordination number r

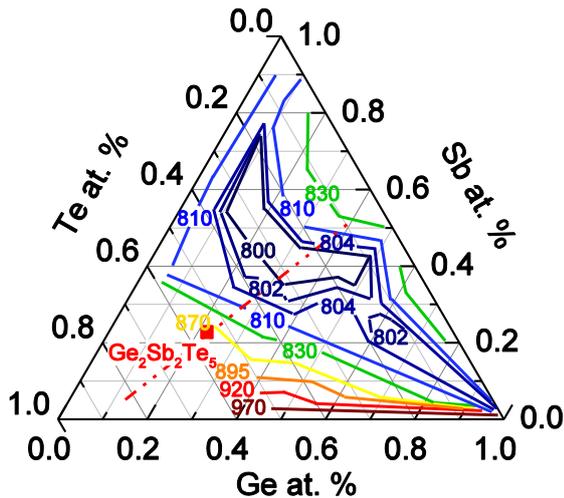


Fig. 7: GeSbTe melting temperature contour plot obtained from references [4,5]

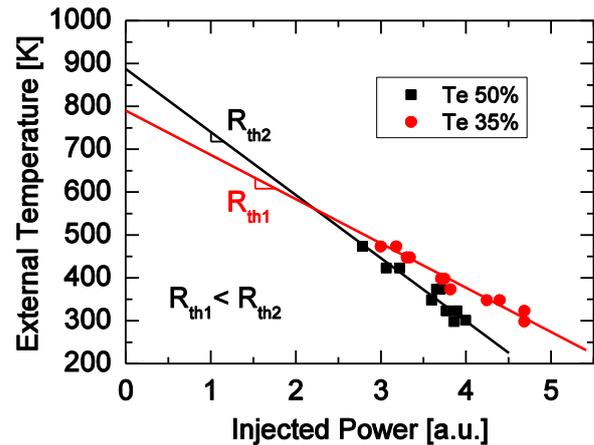


Fig. 8: Extraction of the melting temperature for two alloys with different tellurium content. Higher tellurium content alloy shows a higher melting temperature as expected from Fig. 7.

of the GST material: a material with higher r translates into better retention and higher set current. The dependence of the reset current from tellurium content seems to be not consistent with data reported in the literature where an increase of the melting temperature is expected increasing the tellurium content, as reported in Fig. 7. To better investigate this point, we used the experimental method described in the previous section for cell thermal resistance and GST melting temperature extraction in PCM cells. The method is now based on the observation of the Resistance-Power (R - P) characteristic curves of different alloys as described in the previous section. Results are reported in Fig. 8 for two alloys with different Te concentrations, namely 50% and 35%. The plot evidences on one hand a lower melting temperature extracted for the Te-poor compound, around 800K, consistently with results reported in Fig. 7 [4,5] and on the other hand a lower R_{th} in the Te-poor alloy ($R_{th1} < R_{th2}$). This confirms that despite Te-poor GST having a lower melting temperature, the material itself experiences worse thermal confinement during the phase change operation, thus requiring a slightly higher injection of power to reach its melting condition than the Te-rich counterpart. This is due to a higher thermal conductivity of the Te-poor alloy responsible for the change in the overall thermal resistance of the device.

4. CONCLUSION

In this paper we described a new method for estimating the melting temperature and the thermal properties of chalcogenide alloys in PCM cells. The method allows insights into physical parameters in very small nanostructures where it is usually difficult to collect measurements with conventional methods. The method has been applied to cells based on the so called Wall architecture at 90 nm lithographic node and at a scaled node. In the second part of the paper, we investigated different chalcogenide alloys, exploring GST compositions toward the Te-poor direction, producing effects on both the PCM electrical and thermal parameters. Te-poor alloys show decreased amorphous resistance and enhanced retention capabilities, following the average coordination number metrics. Finally their lower thermal resistance translates into slightly higher power consumption during the phase change operation, even in presence of a decreasing melting temperature reported toward the Te-poor region.

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Biographies

Andrea Redaelli received the Laurea (summa cum laude) and Ph.D. degrees in electronic engineering from the Politecnico di Milano, Italy, in 2003 and 2007 respectively. During the Ph.D. thesis he worked on Phase Change Memories in the Department of Electrical and Electronic Engineering (Politecnico di Milano), collaborating with the Non-Volatile Memory Technology Development Group of the Advanced Research and Development of STMicroelectronics, Agrate Brianza. His research interests include the modelling and characterization of transport properties and phase-change transition of

chalcogenide-based devices. From 2007, he joined STMicroelectronics working on advanced technologies for non volatile memories, being also involved in EU funded projects on emerging memories. Since 2008 he is working on 45 nm PCM technology developments, firstly in Numonyx (the INTEL-ST spin-off for non volatile memories) and then in Micron, following the incorporation of Numonyx in Micron Technology. His work areas include memory array architecture definition, design of test structures and electrical testing. He mainly focused his efforts on electrical performance improvement through process and programming algorithms. From 2005 to 2009, he also cooperated with the Department of Electrical Engineering, Politecnico di Milano, in holding master's classes on electronics and signal conditioning. Andrea is author and co-author of about 30 papers and 20 patents and filed patent applications.

Mattia Boniardi was born in Milano, Italy, in 1982. He received his M.Sc. and Ph.D. degrees in electronic engineering in 2007 and 2011 respectively from the Politecnico di Milano. During his Ph.D. studies he worked on the electrical characterization and modeling of the Phase Change Memory (PCM) technology in the framework of the collaboration between the Electrical and Electronic Engineering Department (Politecnico di Milano) and Numonyx, now Micron Technology. During his studies he was focused on the comprehension of transport and drift mechanisms related to the amorphous state of PCMs and on the chalcogenide material exploration. In 2011 he was hired by Micron Technology where he is currently working toward the 45 nm PCM technology development. He is mainly focused on the electrical characterization of PCM devices for reliability assessment and process optimization. Since 2010 he has been teaching assistant at Politecnico di Milano for bachelor classes on electron device fundamentals. Mattia is author and co-author of about 15 papers and 1 patent application.

Roberto Bez received the doctoral degree in Physics from the University of Milan, Italy in 1985. In 1987 he joined the Central R&D department of STMicroelectronics and started to work on Non-Volatile Memory (NVM) technologies. In the 1990s, he participated in the development of the NOR Flash memory technology, initially as expert of the device physics and reliability and subsequently as project leader of the multilevel product development. Since 2001, he has been working on the development of the NAND Flash memory and on the emerging technology based on the phase change memory concept. In March 2008 he joined Numonyx as Fellow, driving the development of the phase change memory and other alternative NVM technology. From April 2010 he is with Micron, which acquired Numonyx. He has authored many papers, conference contributions and patents on topics related to NVM. He has been lecturer in Electron Device Physics at the University of Milan and in Non-Volatile Memory Devices at the University of Padova, Politecnico of Milan and University of Udine.