Gradual change of resistance on high current density induced by nano-scaled voids in the crystalline phase of $Ge_2Sb_2Te_5$

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ABSTRACT

Electrical failure is first observed in crystalline $Ge_2Sb_2Te_5$, which indicates phase change memory can be failed in the crystalline phase especially non-active region. Resistance of $Ge_2Sb_2Te_5$ increase gradually during current stressing, which can be explained by nano void generation quantitatively. In this study, we investigate the origin of the crystalline failure in $Ge_2Sb_2Te_5$ induced by electrical current to identify the mechanism of degradation.

Key words: Phase Change memory, $Ge_2Sb_2Te_5$, Electromigration, Degradation of Crystalline, etc.

1. INTRODUCTION

Phase change memory (PCM) suffered from harsh operating conditions such as high temperature and current density. These severe conditions can cause reliability problems like void formation or compositional variation, which has been known to current-induced migration called electromigration (EM). There are many previous research about migration behavior of Ge2Sb2Te5 (GST) induced by electric current,[1-2] while most failure mechanism has focused only on liquid phase. As diffusivity of liquid phase is much faster than that of crystalline phase, migration-induced failure have been known to occur in the liquid phase dominantly and crystalline phase has been viewed as the stable state for EM so far.

Here, we discovered a new failure mechanism in crystalline GST, which has never been reported. Despite of low diffusivity of atoms in crystalline phase, resistance of GST increase gradually for long periods of time. This cumulative can affect to instability of SET resistance. Because not all of regions of GST are melted during PCM operation, some regions stay crystalline phase continuously with high current stressing. In crystalline phase, damage evolved by atomic migration is accumulated without recovery through melting. Therefore, accumulated damage generate irreversible change to crystalline phase and can arouse reliability problems. In the present work, we investigate the failure mechanism of crystalline phase of GST using high current biasing and quantitative analysis

2. EXPERIMENTS

The GST line structures with 20 ㎛ in length, 2 ㎛ in width, and 300 ㎚ were made by photo lithography. GST films were deposited by using DC sputtering on Silicon oxide wafer, and annealed for 1 hour at 250 °C to crystallize the initial amorphous phase into hexagonal phase. Line-shaped samples, which had uniform current density and easy structure for quantitative analysis, were used for model study. Direct current (DC) and alternative current (AC) were applied to GST line to confirm the polarity effect. Failure morphology and composition were observed using SEM and TEM.

3. RESULTS & DISCUSSION

We observed the resistance increase continuously for hours at the current density ranged from 1 to 1.5 MA/cm^2. Their morphology had damaged by very small void, which behavior was totally different from our previous result about molten phase failure.[2] Figure 1 shows the resistance results and SEM image of the GST line after the test in DC and AC condition. They have the same condition with current density, so temperature including joule heating must be similar for both conditions. Unlike DC test, neither resistance change nor void generation were observed in AC condition, which means the failure is affected by electrical bias. Consequently, the gradual failure is originated from EM. Voids were generated not only on the surface but inside of GST as shown Figure 2(a) and their average size was about 7 nm. We can calculate the volume fraction of void quantitatively using image analyzer. Because void can be regarded as insulator, generation of voids is related to resistance increase. Calculated volume fraction of void was 0.28, which can explain the increase of resistance quantitatively.

We can propose the mechanism based on defect-induced melting which means locally vulnerable points like defects were melted heterogeneously under melting condition.[3] The origin of defect is expected to amorphization induced by EM. Amorphous phase can be transformed from crystalline phase without melting though EM according to recent paper,[4] which act as defect site. Compositional deviation in voiding spot as shown Figure 2(b) is clear evidence of localized melting. From the phase diagram of GST, GST is not melted congruently and separated two phase during solidification process, one is Ge-rich phase haven relatively low melting point, the other is Sb-rich phase haven higher melting point, respectively.[5] Therefore, void area was once locally molten state and compositional change came up during solidification. Schematic image of the failure procedure is shown in Figure 3.

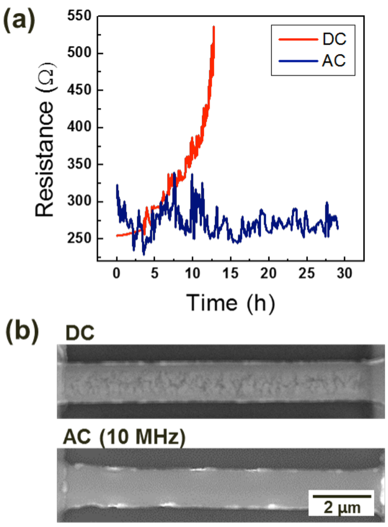

Figure 1 Resistance-time curve under DC and AC current and SEM images after the test

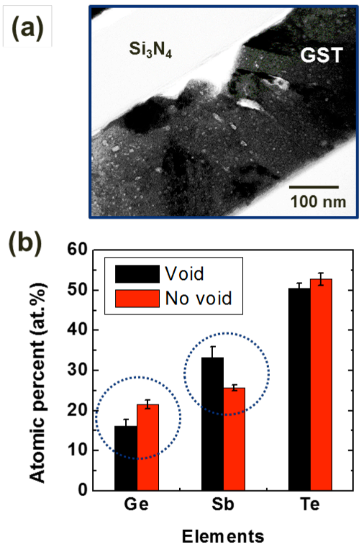

Figure 2 Cross-sectioned TEM image and composition depends on position

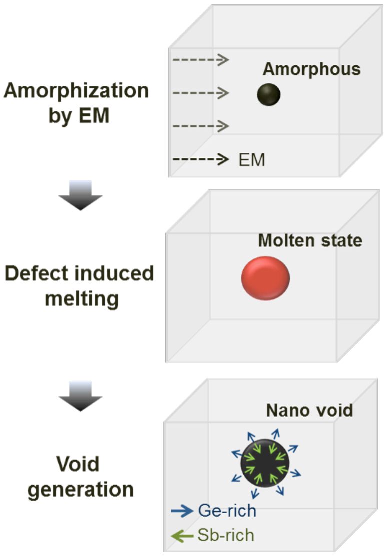

Figure 3 Schematic diagram of mechanism with void generation

4. CONCLUSION

Based on microstructural and compositional analyses, we investigated the new failure mechanism of GST in crystalline phase. Defect-induced melting aroused compositional change in localized area which was nano-sized voids. This failure indicates that devices can be failed by atomic migration in crystalline state as well as in liquid state, which can cause fatal reliability problems even on the intermediate current level that has been considered to be safe against the failures.

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Biographies

Yong-Jin Park was born in 1988 in Busan, Korea. He received his B.S. degrees in Materials Science & Engineering from Seoul National University, Korea in 2010. He has been a doctoral student in Seoul National University since 2012. He and his colleagues Tae-Youl Yang and Ju-Young Cho are currently working on their projects in the group of Dr. Young-Chang Joo. His research topic includes the migration behavior and failure mechanism of chalcogenide materials and reliability problems based on high current density and temperature.