

Effects of SiO₂ inclusions in GeTe based alloys for PCM applications

G. Navarro*, A. Persico, E. Henaff, F. Aussenac, P. Noé, C. Jahan, L. Perniola, V. Sousa, B. De Salvo
CEA, LETI, MINATEC Campus

17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France.

* Corresponding author. Email address: gabriele.navarro@cea.fr

ABSTRACT

We present the effects of SiO₂ inclusions in GeTe-based Phase-Change Memories. We demonstrate a 50% RESET power reduction correlated with the enhanced thermal and electrical efficiency of the cell by SiO₂ addition. Moreover we show the possibility to engineer the threshold voltage (V_{TH}) of the cell at high operating temperature, thanks to the changed crystallization dynamics induced by SiO₂ inclusions into GeTe.

Key words: SiO₂ inclusions, GeTe, Phase-Change Memory.

1. INTRODUCTION

Embedded nonvolatile memories (eNVM) has become a major component of many modern systems. In decentralized and mobile units, they enable autonomous software control and management of an increasing amounts of data [1]. One of the markets with the most stringent specifications is the automotive one, which requires operations from -40 °C up to 175 °C. Moreover mobile applications continuously push memory requirements further, making power consumption optimizations for memory critical [2]. Many efforts have been made in the last years to improve the thermal stability of the PCM cell and to decrease its power consumption. A well recognized cost-effective approach, is to add dopants to increase the stability of the amorphous state [3]. In this context, the effect of SiO₂ inclusions in Ge₂Sb₂Te₅ (GST) based PCM devices has been already reported [4], showing the possibility to reduce the thermal conductivity of the phase-change material increasing the SiO₂ content, with the consequent reduction of the programming power. What makes GeTe alloys more interesting than GST for device application, is the wide resistivity variation, the high crystallization speed, and also the higher crystallization temperature (~ 180 °C) compared with standard chalcogenide materials [5]. In this light, we present the effects of SiO₂ inclusions in GeTe-based PCM devices. Controlling SiO₂ at. % we demonstrate the possibility to engineer the electrical performances and to address high-operating-temperature applications.

2. MATERIAL CHARACTERIZATION

SiO₂-Germanium-Telluride amorphous thin films of 100 nm thickness were deposited on SiO₂(500 nm)/Si substrates by co-sputtering from stoichiometric GeTe and SiO₂ targets. The nominal SiO₂ content as referred to in this paper was varied from 0% to 10%. The 4-probes resistivity measurements shown in **Fig. 1** and performed by annealing the samples up to 350 °C with a constant rate of 10 K/min reveal the increase of the amorphous resistivity with increasing the SiO₂ at. % as well as the increase of the crystallization temperature (187 °C for GeTe, up to 244 °C for GeTe-SiO₂10%). On the contrary we don't observe a remarkable variation of the activation energy of the conduction (correlated with the energy band gap) in the amorphous samples with the increasing of SiO₂ at. %.

The sharp drop in resistivity, once reached the crystallization temperature, suggests that all the materials, once nucleated, exhibit a very high growth speed typical of GeTe [6]. It also suggests that the activation energy, as calculated with the Kissinger method (**Fig. 2**), is in reality the activation energy of the nucleation process and it increases with the SiO₂ content, as already reported for SiO₂-doped GST [7]. Our data confirms the important role of SiO₂ inclusions resulting in a decrease of the nucleation rate and a boosted activation energy of the nucleation.

3. DEVICE ELECTRICAL CHARACTERIZATION

We integrated 100 nm thick GeTe-SiO₂ materials in lance-type analytical PCM devices. To extract the electrical parameters at room temperature and after at high temperatures, we tested 54 devices for each composition with setup measurement and techniques already described in [5].

3.1. THE DEVICE POWER EFFICIENCY - From programming characteristics we can extract the main electrical parameters of the GeTe-SiO₂ devices. **Fig. 3** reveals the increase of the RESET resistance of the devices with increasing SiO₂ content (as already pointed out in Fig. 1). We observe also the decrease of the RESET current (I_R), with a reduction reaching up to 44% for 10% SiO₂. We believe that the increase of the holding voltage V_H , which we extracted experimentally (**Table I**), contributes partially to the reduction of I_R needed to achieve the RESET power, while the series resistive contribution is negligible ($P \cong V_H I_R$). Besides this effect, our measurements also point out a reduction of 50% of the total RESET power. This reduction is more likely due to a better thermal efficiency of the cells, rather than to a decrease of

the melting temperature of GeTe with SiO₂ inclusions. In fact, as reported in [8] we expect a decreased thermal conductivity of crystalline GeTe-SiO₂, as the amount of SiO₂ increases, that could explain the increased thermal efficiency of the cell environment [9]. To check this hypothesis we report in **Fig. 4** the analysis [10] of the thermal resistance (R_{TH}) of 0% and 10% devices, obtained from the electrical characterization of the cells at high temperatures (up to 180 °C). The power (P_M) needed to reach the melting temperature (T_M) of the phase-change material integrated in the cell, is correlated with the annealing temperature (T_A) according to the equation $P_M = R_{TH}^{-1} (T_M - T_A)$. The interpolation of the data, clearly shows a 72% increase in the thermal resistance of the SiO₂10% cells respect to the standard GeTe-based. In Table I we also show that SET state is strongly affected by SiO₂ inclusions: the crystallization becomes slower, as already demonstrated for GST-based materials [11] (longer SET pulses are required), and the tendency of the lowest SET resistance to increase is possibly due to the reduced crystal grain size [7]. However, since both the SET and RESET resistances increase, it allows to preserve a SET/RESET resistance window of about three orders of magnitude. In **Fig. 5** finally we show the unchanged conduction regime in the subthreshold region, for GeTe and GeTe-SiO₂10%.

3.2. AVRAMI ANALYSIS - We report in **Fig. 6** the result of the interpolation by an Avrami equation ($R_{RESET} \propto \exp(-kt^n)$) of the recrystallization curves for three different at. % of SiO₂ contents at 140 °C. We suppose in fact, a time dependency of the RESET resistance (R_{RESET}), dominated by the parameters k and n , correlated with the crystallization dynamics of the phase-change material. The increasing of SiO₂ in the material, lowers the parameter n that can be correlated with the reaction order of the crystallization process. The transition to a diffusion controlled growth rate and the reduction of the nucleation rate can be concurrent and provide the lowering of n , confirming the proposed hypothesis of a changed crystallization dynamics [12].

3.3. THRESHOLD VOLTAGE - The decrease of the threshold voltage V_{TH} with the temperature, results in an increased sensitivity to reading voltages at high operating temperatures [13]. This problem of PCM technology, could make useless all the efforts made to increase the thermal stability of the phase-change material chosen for the target application. We report in **Fig. 7** the variation of V_{TH} as function of the SiO₂ doping content and temperature. As a result, GeTe appears not to be able to sustain a 1 V reading voltage above 60 °C while standard commercial operating temperatures range up to 70 °C. On the other hand, thanks to the increase of V_{TH} with the SiO₂ content, we show that GeTe-SiO₂10% RESET state is capable of a 1 V reading voltage up to 120 °C. Our results highlight the contribution of the changed nucleation dynamics to the increase of the threshold voltage [14].

4. CONCLUSIONS

We presented the effects of SiO₂ inclusions in GeTe-based PCM devices. We demonstrated how the increase of the threshold voltage with the SiO₂ content opens the possibility to engineer V_{TH} for high-operating-temperature applications. This property was correlated with the increase of the activation energy of the crystallization process and the changed crystallization dynamics. Moreover, we highlighted the significant reduction of programming power, following the introduction of SiO₂ into GeTe, which enables addressing low-power applications.

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Biography

Gabriele Navarro was born in 1983. He received the Master degree (summa cum laude) in microelectronic engineering from the University of Padova (Italy) in 2007 with an experimental thesis on the reliability of Phase-Change Memory (PCM) technology in the framework of a collaboration with STMicroelectronics. In 2009 he received the Laurea degree in Physics from the University of Padova (Italy) with an experimental thesis on the variability and signal reconstruction of gamma-ray sources in the framework of the NASA project GLAST. Since 2010, he has been working toward the Ph.D. degree in the Advanced Memory Laboratory in CEA, LETI, MINATEC Campus (France). His current research interests include the engineering, the physical and electrical characterization and the simulation of highly scaled Phase-Change Memory devices. He is author/coauthor of more than ten papers published in international journals and presented in international conferences.

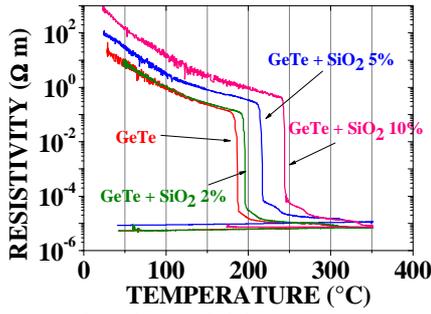


Fig. 1. Temperature-dependent resistivity measurements performed on 100 nm GeTe-SiO₂ thin films. The results reported are for a heating rate of 10 K/min.

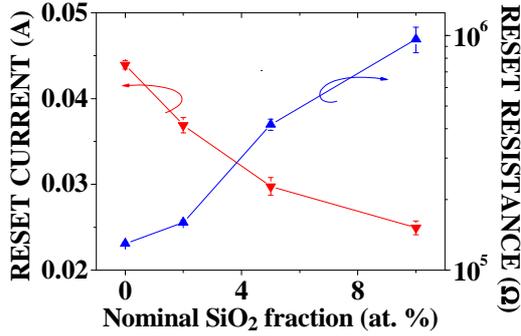


Fig. 3. Trend of RESET current and RESET resistance for all the at. % of SiO₂ under test.

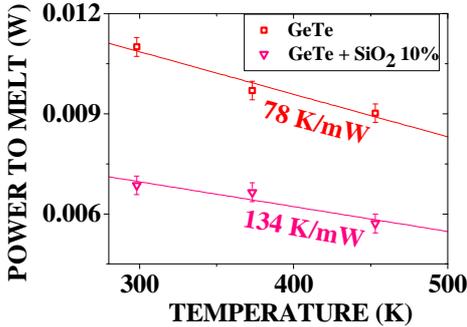


Fig. 4. Thermal resistance (R_{TH}) extraction for GeTe and GeTe-SiO₂10% devices. The SiO₂ doping increases the thermal resistance of the devices, providing a better thermal confinement.

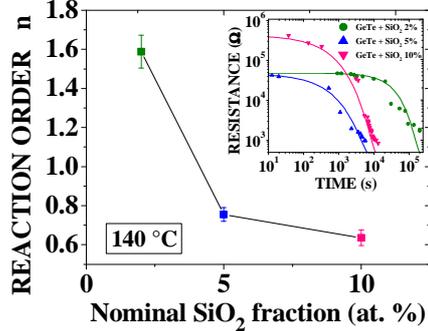


Fig. 6. Interpolation of the curves obtained from recrystallization of the devices at 140 °C (inset): it allows to calculate the reaction order n , here as function of the SiO₂ content. The decreasing of n as the SiO₂ content increases, is the evidence of a crystallization process affected by the inclusions.

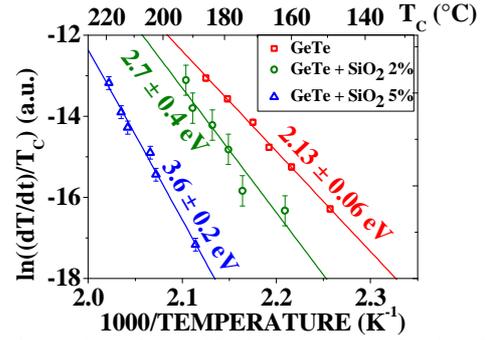


Fig. 2. Kissinger plots of crystallization temperature for the 100 nm thin sheet of GeTe with 0, 2 and 5 at. % of SiO₂. The activation energy of the crystallization, increases with the content of SiO₂.

SiO ₂ (at. %)	V _H	MIN SET Time Width	MIN SET Resistance	RESET Power
0%	0.33 V	50 ns	134 Ω	22 mW
2%	0.34 V	60 ns	459 Ω	20 mW
5%	0.51 V	100 ns	795 Ω	16 mW
10%	0.65 V	500 ns	4.01 kΩ	11 mW

TABLE I. Electrical parameters: holding voltage (V_H), minimum SET pulse width (to reach the minimum SET resistance), lowest SET resistance and RESET power for the four composition under test.

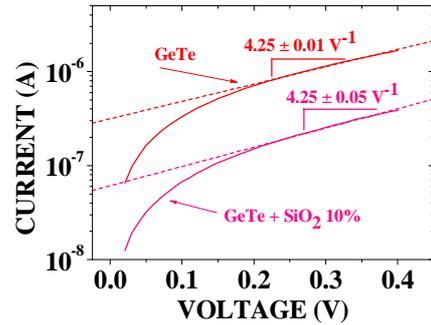


Fig. 5. I-V characteristics at room temperature for GeTe and GeTe-SiO₂10% devices. The two subthreshold slopes has a confidence level of 100%, calculated on a population of 100 cells for each compositions.

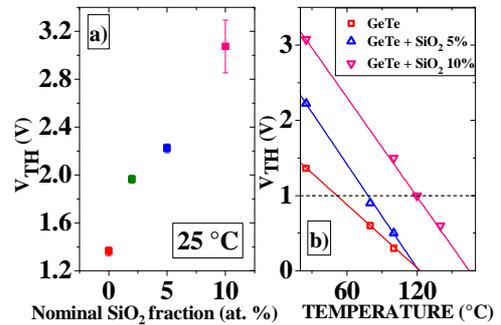


Fig. 7. a) Threshold voltage as function of the SiO₂ content at room temperature. b) Behavior of the threshold voltage in temperature, for different at. % of SiO₂. The doping increases the immunity of the RESET state to standard reading voltages at higher operating temperatures.