Advances in Phase Change Memory Technology

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ABSTRACT

Phase Change Memory is one of the best candidates for next generation non-volatile memory which can enlarge its applications segment, due to improved performances, and can fulfil the requirements for future down-scaling. Thermal, electrical and geometrical aspects controlling the functionality of a chalcogenide-based phase change memory cell are analysed. Processing condition effects, material properties and compatibility issues are investigated. Novel cell geometry, based on a μtrench approach, fully compatible with an advanced CMOS technology is presented. Sustainable programming currents, long cycling endurance and long-term data retention capabilities have been demonstrated for multi-megabit arrays.

Keywords: Non-volatile random access memory, phase change memory, chalcogenide, high density memory

1. INTRODUCTION

General expectations for future memories can be summarized as non-volatile, fast, low energy, high density and long endurance, mainly driven by the growing demand for electronic portable equipments with extended performance. Although Flash memory technology, based on the floating-gate concept, has been able to follow the evolution of the semiconductor roadmap[1], some physical limitations could be critical for reliable downscaling beyond the 65 nm node. Moreover a finer write granularity, compared to the block erasing of Flash memory, together with higher speed and endurance, could extend the Non-Volatile Memory (NVM) capability and simplify the memory structures of several equipments. Ideally, the need is for technologies that combine higher density with the fast read/write speeds of synchronous RAM, the lower cost of dynamic RAM, and the nonvolatility of Flash memory, which can store data when a device is turned off.

	DRAM	Flash	FRAM (ferroelectric)	MRAM (magnetic)	PCM (phase change)
Relative bit size 1= DRAM cell size (~NOR Flash)	1	0.25 - 1	3 - 10	1 - 3	0.5 - 2
Relatv. mask count	1	1.1	1	1	1
Scalability	Fair	Fair	Poor	Poor	Good
Endurance	Unlimited	10^5 Block erasing	10^{10} destructive read	$>10^{14}$ Sensing critical	10^{12}
Data retention	10ms	> 10years	> 10years	> 10years	> 10years
Write time	< 100ns	μs/ms	< 100ns	< 100ns	< 100ns
Write power/B (Vxl)	3Vx100μA	5V x 1mA	3Vx100μA	1.8Vx10mA	3Vx1mA
Maturity	Volume prod.	Volume prod.	Limited prod.	Test chips	Test chips

Table I: Memory Technology Benchmark

Among alternative NVM concepts like F-RAM and M-RAM, that have been under investigation since a few years, Phase Change Memories (PCM) have more recently received sustained interest, since their early proposal[2,3] in late '60, and now are considered one of the best candidates for next generation NVM, due to improved performances compared to Flash (access time, read throughput, direct write, bit granularity, endurance) as well as to their good scalability within current CMOS fabrication methodology[4-7] (table I).

2. PHASE CHANGE TECHNOLOGY CONCEPT

PCM, otherwise called Ovonic Unified Memory (OUM)[8], is based on the rapid reversible phase change effect in some materials under the influence of an electric current pulse.
Phase transition technology has been in use for several years in non-volatile applications such as optical disks; for that application the difference in optical characteristics (reflectivity) between crystalline and amorphous states defines the

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logic state of an individual bit, whereas for PCM applications it is the resistance of the cell that is measured; for optical disks the phase transformation is driven by the energy of light pulses, whereas for PCMs is the Joule effect produced by the electrical current that provides the heating for transitions.

Basically the PCM cell consists of a PC material layer embedded in a dielectric structure and in contact with two electrodes. Along the conductive path of the cell a small volume in the phase change media acts as a programmable reversible series resistor with low-field resistance that can change up to 3-4 orders of magnitude, depending on the material phase state: crystalline (low resistance) or amorphous (high resistance), corresponding to logic states 1 and 0, respectively. The information is therefore stored in the structural state of the material itself.
For current driven transformation, the switching between the low conductive to the high conductive state has an electronic origin[9, 10], but the material transformation is still completed (as for the optical case) by means of local temperature increase. To drive the phase change alloy to the amorphous state (RESET operation), the temperature must be increased above the melting point followed by a rapid quench to temperatures low enough to prevent the crystallization and to stabilize a disordered state. If the material is heated at a temperature below the melting point but high enough to promote crystal nucleation and growth, its crystalline phase is stabilized (SET operation).
Following this phenomenology, three bias (current) levels correspond to READ, SET, RESET operating points, where the lower is just for read out and should not produce any heating nor thermal disturb, whereas the other two are tuned in order to produce intermediate and high heating, corresponding respectively to crystallization and melting of the phase change material (fig. 1). The special combination of the PC material properties (electronic switching, amorphous meta-stability, fast crystallisation) makes possible the reversibility between the two states.

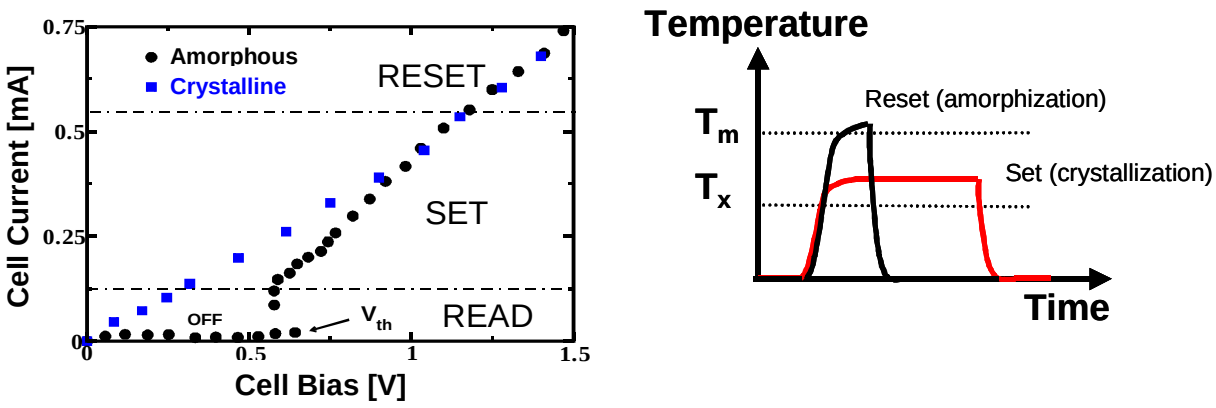


Fig. 1: a) Typical I-V characteristic of a PCM cell: V_{th} identify the electronic switching threshold;
b) qualitative temperature behaviour of the phase change active region corresponding to reset and set pulses.

In order to form a functional compact cell array, a PCM must consist of a variable resistor (data-storage phase change cell) in series with a selector device (transistor). The basic PCM cell has a 1T/1R structure. The type of transistor and of data-storage (geometry, size) depends on the application and on the process constraints.
For high-density memory, the vertical integration with a *pnp* bipolar transistor enables a more compact layout and better current driving capabilities, but it requires a dedicated process for the BJT device in a standard CMOS flow. For low cost embedded memory the selector is a n-channel MOS, which is easily integrated with a minimum overhead of masks; in this case the cell size is not a severe constraint.

3. PCM PARAMETERS ADDRESSING

The wide experience developed on phase change materials for optical application suggested the materials to be more suitable for PCM. In fact, OUM generally comprise layers of chalcogenide semiconductor thin-films containing at least one group-VI element, which have the basic material properties to enable PCM functionality: good thermal stability of the amorphous phase at room temperature, fast crystallisation, relatively low melting temperature, single phase transition, good contrast between amorphous and crystalline state. In particular, the alloy $Ge_2Sb_2Te_5$ (GST) is nowadays the reference material for PCM application. The most important physical-chemical characteristic of PC material is the

great availability of weakly bounded electrons (mainly from the group-VI elements lone-pair orbitals) and the strong similarity between the atomic local structures of the crystalline and the amorphous phases, again related with the presence of lone-pairs which control the local atomic configuration.
Nevertheless, PCM applications have different constraints compared to optical ones: different heating mechanism, different geometry, different boundary materials (CMOS compatible), more severe power limits, extended endurance, long term data retention at relative high temperature, which require extensive parameter optimisation and stimulate to extend the investigation to modified GST or to other phase change materials.
Table II gives an overview of the main control parameters of PCM functionality.
The most severe constraint has been identified as the amount of electrical current necessary to RESET the PC cell. This factor limits the size of the selector (transistor) which has to provide the current and puts limits also on the circuitry (contacts, bit lines, dielectrics, ...), thus impacting the overall device size and limiting the achievement of low cost, high-density memory.

Table II: PCM parameters addressing

Issue	Control Parameter	Physical	Possible solution
RESET current	Geometry/Size	Current confinement (high local power) Transition volume Thermal confinement	Reduction of contact area and active volume; PC thickness, electrode size
	materials properties		
	PC Tmelt	Reduction of required heating power	
	PC electrical resistivity	Increase local heating power	N doping, …
	PC thermal conductivity	thermal confinement	
	electrode electrical resistivity	heating efficiency	Control material design
	electrode thermal conductivity	thermal confinement	
	dielectric environment	thermal confinement	
Data retention	RESET level condition	Electrical percolation/crystallisation	Amorphous volume, fast quench
	Amorphous meta-stability	Crystallisation temperature Activation Energy	PC doping
	Dielectric materials	Heterogeneous nucleation	optimised cell/material design
Endurance	PC single phase (no segregation)	PC transition properties stability	
	PC/electrode interface stability	Electrical contact stability	Clean interface & chemically stable
	electrical current density	Electromigration	Lowest current density by optimised size/materials/geometry
	electrode thermal stability	electrode el./th. properties stability	
Scaling	RESET current required Current driver type & size	Transistor/circuit scaling	Device power match optimisation
SET resistance	PC/electrode interface	Good & stable contact required	Optimised process (etching, thermal budget, contamination, ..)
Speed	Fast crystallization	Local atomic structure Crystallisation temperature Activation Energy	Others phase change materials (Sn, Bi doping; …)
		Heterogeneous nucleation	optimised cell/material design
	SET pulse profile	Nucleation/growth kinetics	SET pulse optimisation

The RESET current depends, at least, on the heating required to reach the PC melting temperature, which for GST is around 620°C. Since the heating is produced by the Joule effect, the more efficient way in terms of power is to produce it into the same region to be transformed, i.e. into GST. In this case, as a rough approximation, the local power density depends by the current density into GST and by its electrical resistivity. High current density can be achieved forcing the current through small GST cross section defined by the cell geometry. Figure 2 shows two schematic axisymmetric PCM cell structures, as extreme examples where the current is confined by the electrode or by the GST itself, respectively for case *a)* and *b).*

The temperature distributions simulated at the current level corresponding to I_{melt} (the minimum current to obtain a GST fully melted region along the PCM conductive path) give an idea of the different behaviours corresponding to the two different cell structures (Fig. 2). Case *b)* compared to case *a)* requires less current to melt because the high density current path inside the GST is longer, with the result that the GST volume that contributes to heat generation is larger. Moreover, the heated region has a better thermal confinement by the GST itself, which is a bad thermal conductor. All the simulation results presented in this paper are obtained by Finite Element Modelling (FEM) with fixed material properties. Therefore, they have to be considered as qualitative PCM behaviours.

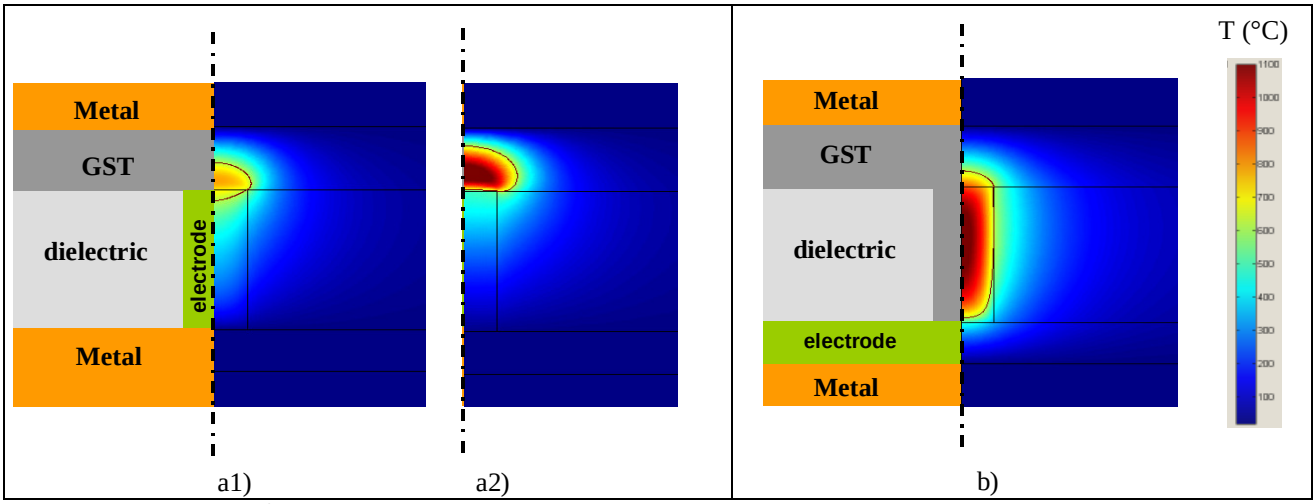


Fig. 2: Basic scheme of PCM axisymmetric cell structure: pillar-like (a), pore-like (b) and corresponding simulated temperature distribution at their respective Imelt; the highlighted isothermal lines are T=620 °C.
a1) and a2) correspond to low and high conductive (thermal and electrical) electrode, respectively.

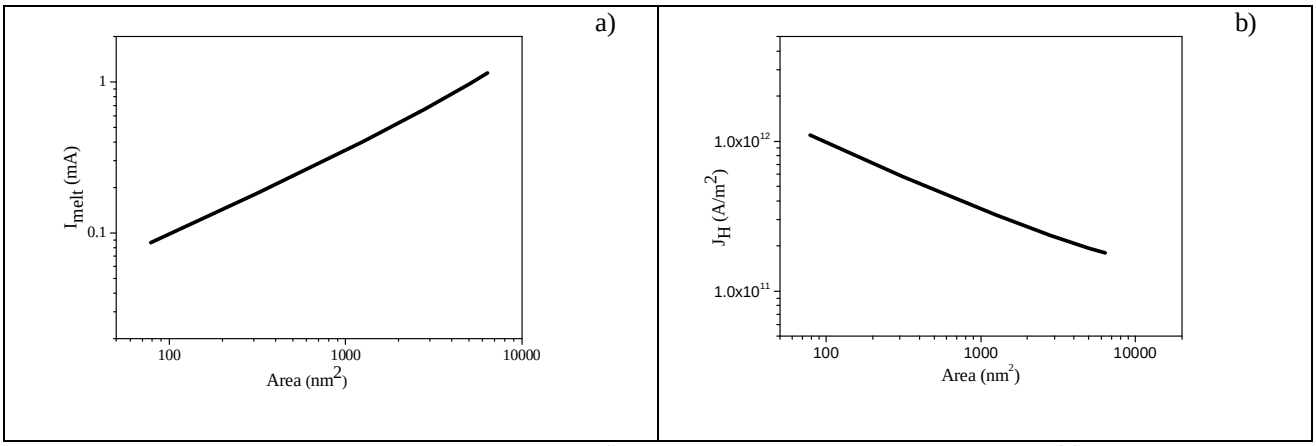


Fig. 3: a) Imelt vs electrode/GST contact area for PCM axisymmetric cell structures (case *a* of figure 2);
b) Current density vs electrode/GST contact area

Figure *3a* indicates the decreasing of I_{melt} with electrode scaling as simulated for axisymmetric PCM structures.
With the present process technology it is sill more reliable to control the current density through the electrode/GST contact area, by the design of sub-lithographic electrode, fabricated using standard processes within CMOS technology (Fig. 2*a*), but further process technology progress could enable the design of cell configuration which takes fully advantage of electrical and thermal confinement.
An alternative approach to obtain small contact area is represented by the μ-trench structure, through the intersection of a thin vertical electrode film and a GST layer deposited into a sub-lithographic trench (fig. 4 and paragraph *4.*).

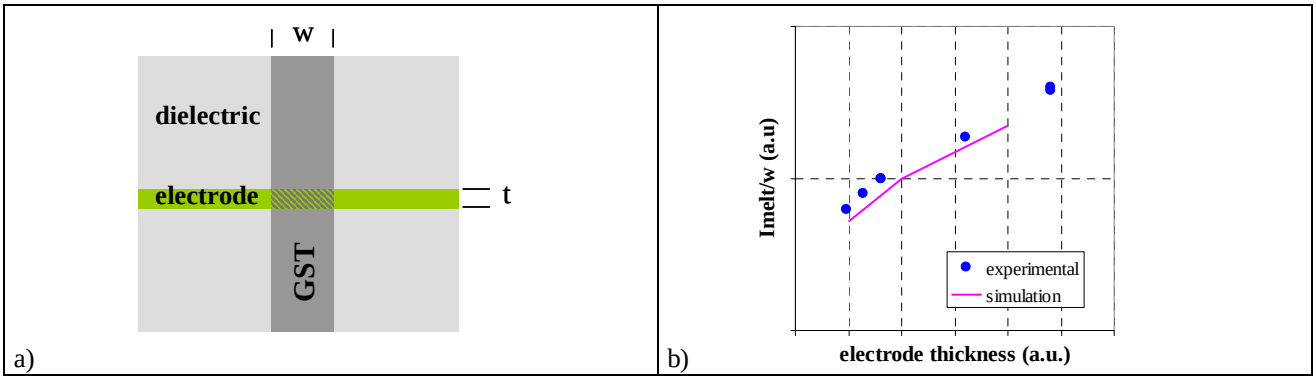
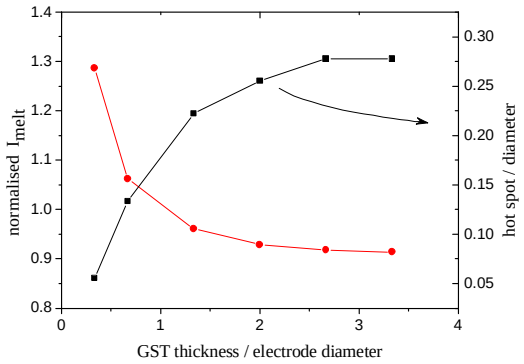


Fig. 4: a) Top view of the μ-trench PCM structure; the shaded area corresponds to the electrode/GST contact; b) Experimental and simulated I_{melt} normalised to trench width (*w*) vs electrode film thickness (*t*)

The thermal confinement of the heated region has also a strong impact on the RESET current, mainly because a good thermal insulation reduces the power required for melting, but there are also some other issues related to the thermal profile and the maximum temperature achieved, which can have impact on the reliability of the materials close to the hot region (PC, electrode, dielectrics). The simulations in Figure 2 (*a1* and *a2*) show, for example, how the electrode transport properties can produce different temperature distributions: higher conductivity (thermal and electrical) requires higher current, produces higher local temperature to achieve the melting of the active region and the hot spot localisation moves more inside the GST.
A hybrid PCM structure based on a partially recessed electrode filled with GST could combine the benefits of current confinement and thermal insulation (case *b*) within a configuration more compatible with CMOS processes (case *a*).



Another parameter which can improve the thermal confinement is the GST thickness, taking the advantage of the low thermal conduction properties of the PC material, as indicated by the result of FEM simulation shown in figure 5 for axisymmetric PCM structures (case *a* of figure 2): I_{melt} is reduced to a minimum level (depending mainly on the electrode conduction properties) if the GST thickness is at least equal to the electrode diameter; also the hot spot position stabilises to a maximum distance from the electrode.

Fig. 5: Simulated normalised I_{melt} and hot spot localisation vs the ratio between GST thickness and electrode diameter (axisymmetric structure)

The thermal confinement plays also a role in PC material cooling to ensure GST quenching to the amorphous state. The thermal time constants of the materials involved seem not to be a problem for future structure scaling.
Since the *surface/volume* ratio of the heated region increases with geometrical scaling, higher power density is required to achieve the same local heating level, balancing the increased thermal dissipation. As a consequence a very high current density should be necessary (around 10^{12} A/m^2), promoting some related critical issues like the electromigration of electrode or GST atoms, which could limit the device endurance. Figure 3*b* shows the increase of the current density corresponding to the I_{melt} required for different axisymmetric simulated PCM cells with scaled electrode size.
Since very small contact area could introduce some limitations on the reproducibility of billions of bits, other approaches have to be also considered to generate high power density, as the increasing of the PC material resistivity, by, for example, nitrogen doping[11]. Figure 6 shows the simulated I_{melt} dependence versus the GST electrical resistivity.
Data retention is another important factor for PCM devices, to take full advantage of the non-volatile characteristic. Since the percolation conduction mechanism has a non-linear relationship with the crystalline fraction, data retention depends not only by the PC material crystallisation factors but also by the statistics and by the topology of crystals

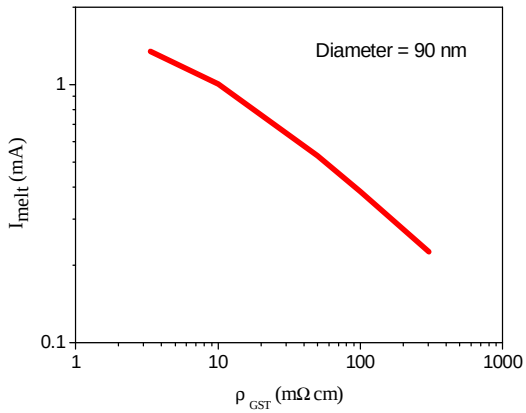


Fig. 6: Simulated normalised I_{melt} vs electrical resistivity; axisymmetric structure with electrode diameter of 90 nm.

distribution, together with cell geometry, RESET condition and crystal nucleation properties of the GST boundary material interfaces.

Since the active region is subjected to severe electrical and thermal condition, it is important to utilise electrodes and surrounding materials with high chemical and thermal stability, in order to preserve their functional properties for long operative lifetime.

The contact area between the electrode and the GST can be considered as the most critical region of the PCM cell. The control of the GST/electrode interface (dimension, cleanness, adhesion, chemical and thermal stability, stress) is a primary issue to guarantee a reliable PC cell functionality on very large arrays. Any contamination in GST bulk and at the electrode interface must be avoided by careful processes optimisation (deposition, etching, thermal budget, …).

Since the crystallisation transformation leads to an ordered lattice, the SET operation takes longer time compared to the amorphisation (RESET). If high data rate are required, a first increase of the write speed can be achieved by the optimisation of the SET pulse profile in order to match the nucleation & growth kinetics of the PC material. Further crystallisation speed is under investigation also for optical data storage using modified phase change materials[12] (Sn, Bi doped).

Finally, the success of PCM development depends on the implementation of process conditions fully compatible with CMOS technology.

4.1. μ-TRENCH ARCHITECTURE

The basic idea is to achieve low programming current maintaining a compact vertical integration through the design of geometry with improved current and thermal confinement. A very low contact area can be achieved by the intersection of a thin vertical semi-metallic electrode with the GST layer confined into a horizontal and perpendicular "μ-trench" [7].

Fig. 7 shows schematic drawings of the cell structure along X and Y directions and their corresponding STEM-TEM cross sections.

Since the μ-trench can be defined by sub-lithographic techniques and the electrode thickness by film deposition, a very small contact area can be achieved (today in the range 1000 – 5000 nm^2), still maintaining a good CD control.

Moreover, the heating efficiency is improved by the electrical current confinement in the GST along the X-direction of the μ-trench.

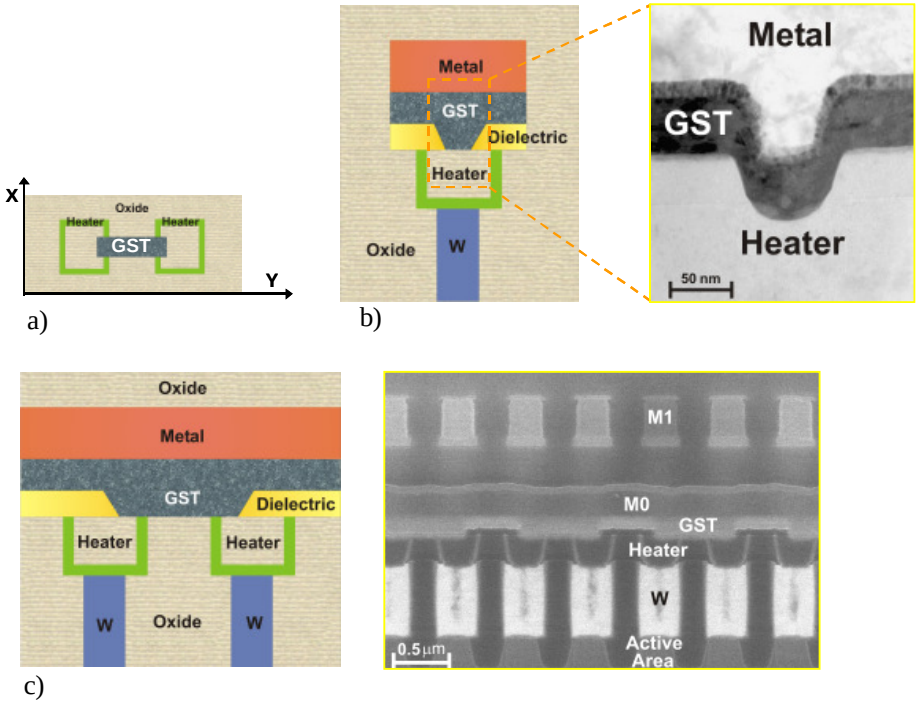


Fig. 7: a) μ-trench scheme top view; Schematic and STEM-TEM cross section along X (b) and Y (c) directions.

The combination of the "μ-trench" data-storage element and a *pnp*-BJT selector makes possible a compact layout ($10F^2$), with a cell area of 0.32 μm^2. The μ-trench PCM cells have been integrated into an advanced 0.18 μm CMOS process.

4.2. ELECTRICAL MEASUREMENTS

The characterisation of the μ-trench PCM cell has been performed by recording the RESET and SET programming pulses followed by a read-out pulse. RESET state (amorphous, high resistance) can be achieved with a 40 ns pulse, while SET state is limited by the crystallisation process which, in this case, requires a pulse in the range of 100 ns. A reliable difference of two orders of magnitude between the SET and the RESET resistance can be achieved using a RESET programming current of 600 μA (Fig. 8).

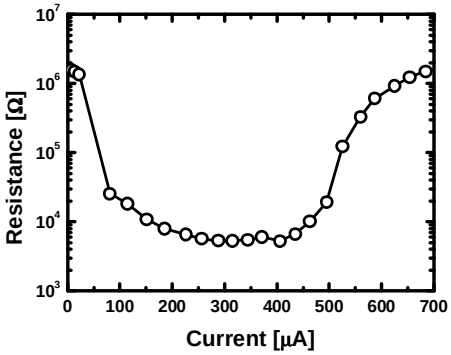


Fig. 8: PCM programming curve (R-I) from the RESET state.

4.3. RELIABILITY & REPRODUCIBILITY

The endurance has been tested and a good programming window is maintained up to 10^{11} cycles (Fig. 9).
From an assessment of the data retention capability, an activation energy of 2.6 eV was determined, thus making possible data retention up to 10 years at 110 C (Fig. 10).

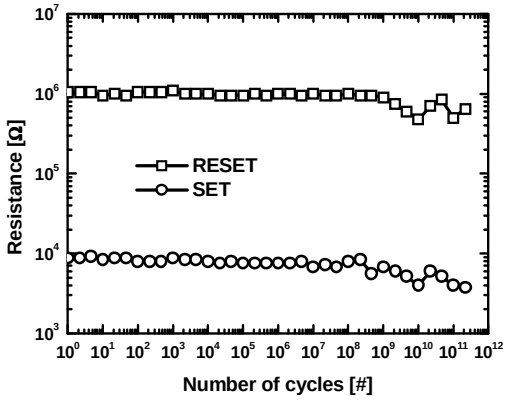


Fig. 9: PCM cycle life.

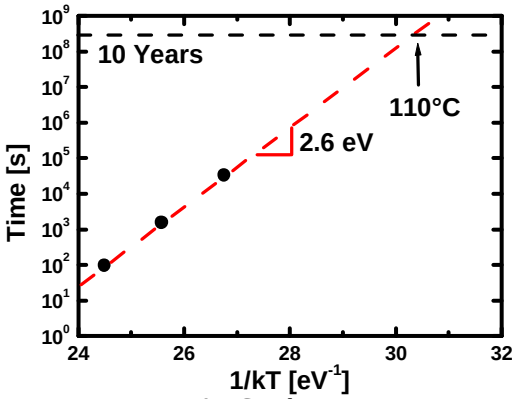


Fig. 10: PCM data retention.

The reproducibility of the cell functionality has been proven by sharp SET and RESET resistance distributions measured on wafer (Fig. 11).
An 8Mbit Demonstrator has been developed and tested. The current distribution after RESET and SET operations is shown in Figure 12, demonstrating a current window suitable for high density arrays.

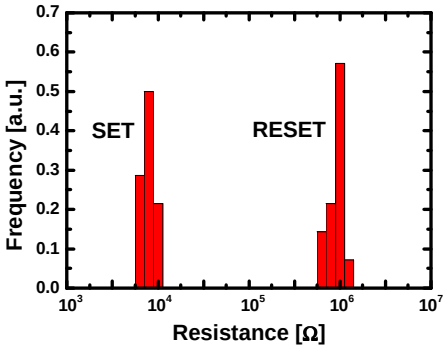


Fig. 11: Distribution on wafer of SET and RESET resistance.

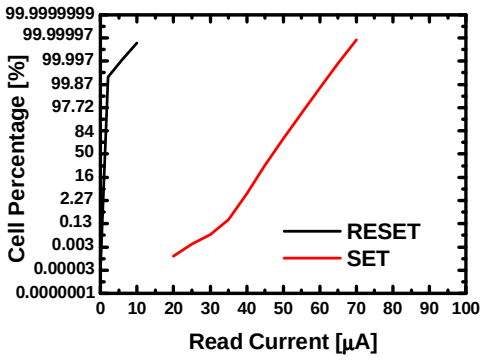


Fig. 12: Distribution of RESET and SET read-out currents for an 8Mbit array

5. CONCLUSIONS

PCM can be considered one of the best candidate for alternative future NVMs, which could extend their application segment with improved performance and higher density.

Several parameters have been identified as controlling factors for optimised PCM functionality, further exploration of their effects will provide better understanding of their impact and correlation.

At the moment the RESET current is the most severe constraint for PCM development: low and reproducible values are required to guarantee compact cell size, low power consumption and reliable endurance.

The reliable integration of the PC chalcogenide into a CMOS process in a large array is one of the main challenges to drive PCM technology to very high density NVMs. Process conditions have to be optimised in order to avoid the negative effect on the PCMs functionality and to improve their reliability: contamination, delamination, thermal budget,… .

A novel μ-trench vertical PCM cell has been integrated into an advanced 0.18 μm CMOS process, demonstrating programming current of 600 μA, endurance of 10^{11} cycles and data retention capabilities for 10 years at 110 C.
Although today PCM technology is still in the learning period, the understanding and the control of some critical parameter, demonstrated also on 8Mbit arrays, are encouraging further development and foreseeing future progress.

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