Investigation on non-rotating and non-volatile phase change memory

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Abstract

In this work, the thermal and electrical performances of chalcogenide-based phase change memory cell were investigated. We have investigated the current reduction issue for CRAM cell theoretically and experimentally. It was found that the value of programming current is highly dependent on the materials and device structure. The effects of materials and cell geometry, structure, and size on thermal and electrical properties of memory cell were simulated and analyzed. The dependence of the memory cell performance on the configuration of memory medium and the cell size were also studied by means of simulation and experiments. An effective method has been proposed to predict the RESET and SET programming current for memory cell. A new structure phase change memory cell was proposed, fabricated and tested. The measurement showed that the memory cell could work at low current.

1. Introduction

With the increasing demand for portable products and large memory arrays for mass storage, the demand for nonvolatile memory (NVM) has been greatly increased these years and will continue further. The desired NVM attributes are high speed, high density, low cost, nonvolatile and easy to integrate. However, today's mainstream memory technologies each have limitations. Driven by the market and application needs, a recent flurry of activity in the development of new NVM technologies has emerged, such as Magnetic Random Access Memory (MRAM), Ferroelectric Random Access Memory (FeRAM) and Chalcogenide Random Access Memory (CRAM). CRAM is considered as one of the best candidates for the next-generation NVM due to its near-ideal NVM advantages: fast access time, low power, low cost, long endurance, high scalability and good data retention [1,2].

CRAM, also known as OUM (ovonic unified memory), is based on a rapid reversible phase change effect in some materials under influence of electric current pulses. The CRAM uses the reversible structural phase-change in chalcogenide material, which in turn changes the electrical resistivity of the material as the data storage mechanism. The small volume of active media acts as a programmable resistor between a high and low resistance with several orders difference. 1's and 0's are represented by crystalline and amorphous phase state, separately. The most significant advantage of CRAM technology is its high scalability. Since the energy required for phase transformation decreases with cell size, the write current scales with cell size, thus facilitating memory scaling.

Currently one of the research focus for CRAM is to reduce the programming current to the level that is compatible with the minimum MOS transistor drive current for high-density integration. The programming current of CRAM, especially the RESET current, is substantially high due to heating and overheating of a cell by repeated write cycles. The programming current scales with the contact area and improves with lithography scaling [3]. Besides the scaling, material engineering and device structure engineering have also been approached to reduce the programming current. In this work, we have investigated the current reduction issue for CRAM cell theoretically and experimentally. It was found that the value of programming current is highly dependent on the materials and device structure. An

effective method has been proposed to predict the minimum programming current. A new structure phase change memory cell was proposed to reduce programming current.

2. Simulation

The phase change in CRAM cell is induced by Joule heat generated by electrical pulses. How to manage the thermal distribution inside the memory cell becomes critical for device performance. It is important to calculate the temperature distribution in a memory cell with different materials, cell geometry, structure, and feature size since such information is helpful for compare the memory performance and optimize the structure. In our thermal simulation work, the temperature distribution was simulated by three-dimensional finite-element method (FEM) and then the thermal expansion was calculated based on the temperature change.

Figure 1 is the schematic view of the CRAM cell structure used in simulation. It has a standard sandwich structure. In this structure, TiW and TiWN were used as electrodes, ZnS-SiO2 as dielectric layers and GeSbTe as a phase change layer. In this simulation, properties of the materials are assumed to be independent of temperature. Heat is mainly generated in the phase change layers. The thermal transfer obeys the standard heat conduction equation:

$$\nabla \bullet k\nabla T + Q = \rho c \frac{\partial T}{\partial t} \qquad (1)$$

where, $\nabla\rho\delta$ is the gradient operator; k, the thermal conductivity; c, the specific heat; ρ , the density; t, the time; T, the temperature and Q, the Joule heat per unit volume and per unit time, which is called heat density. Our model can be simplified into a static magnetic analysis since the voltage applied to the electrodes maintains unchanged. In the static field analysis, the Joule heat density distribution can be expressed as:

$$Q = \frac{1}{n}\sum_{n=1}^{n}[\delta]\{J_i\}\{J_i\} \qquad (2)$$

where, n is the number of integration points, $[\sigma]$ is the resistivity matrix and $\{J_i\}$ is the total current density in the element at integration point i.

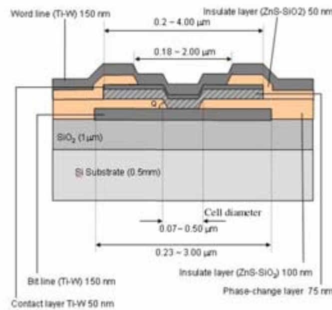


Fig. 1 Schematic cross-section of CRAM cell

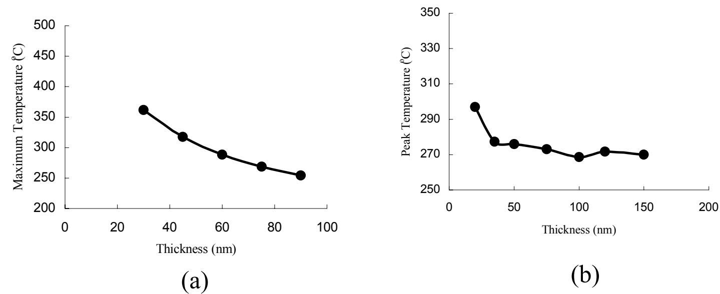


Fig. 2 Peak temperature distribution for different (a) phase change layer thickness (feature size 22.5nm) and (b) dielectric layer

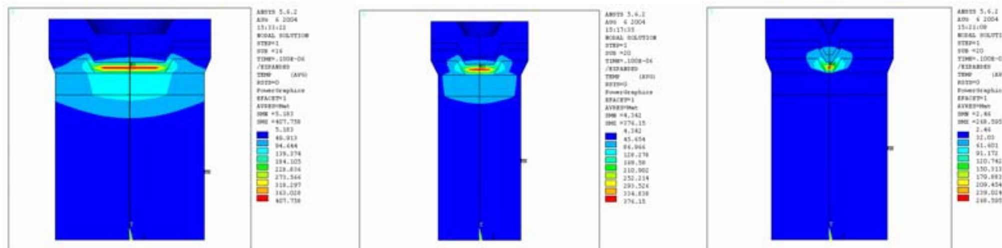


Fig. 3 Temperature distribution for CRAM cell with different radius (a) 245 nm, (b) 100 nm and (c) 22.5 nm

The simulation results show that the temperature distribution is highly dependent on material properties and structures. Fig. 2 presents one of the simulation results, which illustrates the maximum temperature achieved for memory cell with different phase change layer thickness and dielectric layer thickness, respectively. Fig. 2(a) shows that the peak temperature decreases with the phase change layer thickness. Fig. 2(b) shows that when the dielectric layer 1 is above some thickness, there is less variation effect towards peak temperature.

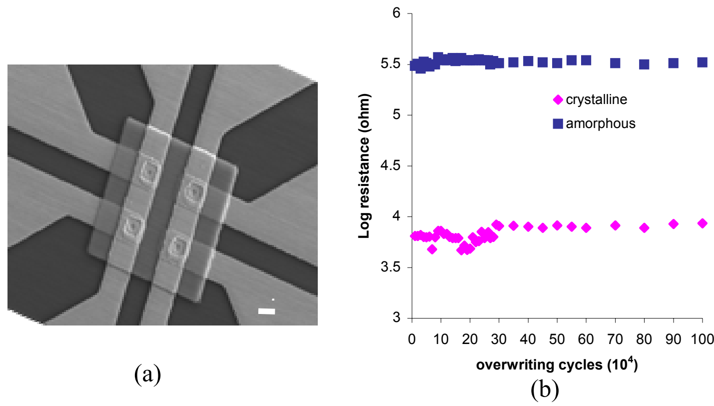
The scaling effect towards the CRAM device performance has also been studied by simulation. The temperature distribution in memory cells with different feature was systemically simulated. Fig. 3 illustrates the cross-sectional view of the temperature distribution for CRAM cell with different feature size at the same pulse amplitude and width. The feature sizes are 245 nm, 100 nm and 45 nm, respectively. It can be clearly seen that the heat is mainly generated and accumulated in the center of the phase change layer. When the cell size reduced, the heat generation and accumulation region was also shrink. No lateral thermal diffusion was observed in memory cell with small size than with larger cell. It confirmed that the energy required for phase transformation decreases with the cell size. Hence, programming current is reduced with the size scaling.

3. Experiments and Results

The memory cells with the above-mentioned sandwich structure were fabricated and tested by a self-developed testing system. During testing, the memory cells were switched between high resistance and low resistance states by electrical pulses. SET process was performed from high resistance state to low resistance state and RESET process was performed from low resistance state to high resistance state. The electrical pulses were applied with varied pulse width and programming current. Figure 4 (a) shows the SEM image of CRAM cell. The cells perform good memory characteristics, e.g. good cycling capability shown in Figure 4(b).

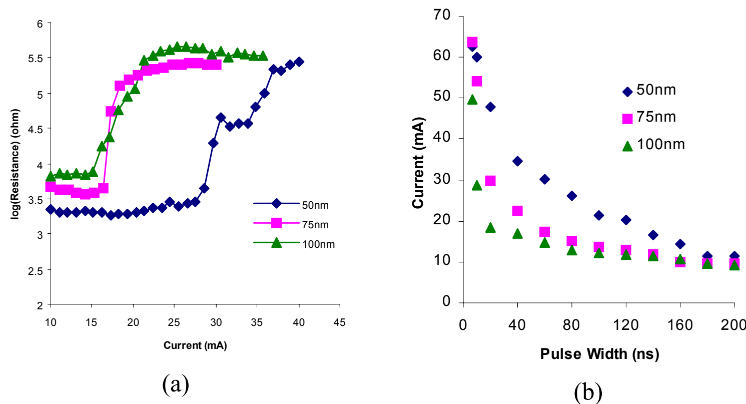
To compare the cell performance, different materials, film thickness and cell size have been investigated. Figures 5 and 6 show some of the results for CRAM cells with different phase change layer and dielectric layer thickness, respectively. The memory cells for layer thickness comparison were fabricated with 1 μm feature size. $Ge_2Sb_2Te_5$ and SiO_2-ZnO_2 were chosen as the phase change and dielectric materials. Fig. 5(a) and Fig. 6(a) plot the curves of resistance versus RESET programming current (R-I) with same pulse width. The curves show that the resistance of the memory cell jumps from low to high value when the programming current is above a threshold value. In this paper, this threshold current is referred as RESET programming current, and the same definition is applied to SET programming current. Memory cell with different layer thickness has different RESET current. In this experiments, the RESET current for the memory cell with 100 nm phase change layer thickness is the lower than with 50 nm and 75 nm; and the RESET current for the memory cell with 80 nm lower dielectric layer thickness is lower than with 100 nm.

Fig. 5(b) and Fig. 6(b) exhibit the curves of RESET programming current versus pulse width (I-W). It was observed that the RESET current is highly dependent on pulse width. In general, lower current is required when the pulse width is longer. It can be clearly seen that there are two regions in the graphs. At the region with long pulse width, the programming current is relatively independent on the pulse width. Beyond that pulse region, the programming current increased sharply when the pulse width reduced.



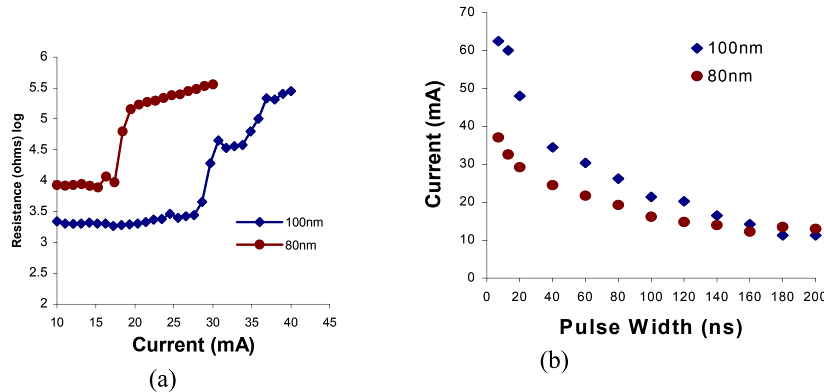
(a) (b)

Fig. 4 (a) SEM image of memory cell and (b) Cycling behavior of memory cell without failure



(a) (b)

Fig. 5 (a) R-I plot with crystalline background for CRAM with different phase change layer thickness, and (b) RESET programming current as a function of current pulse width

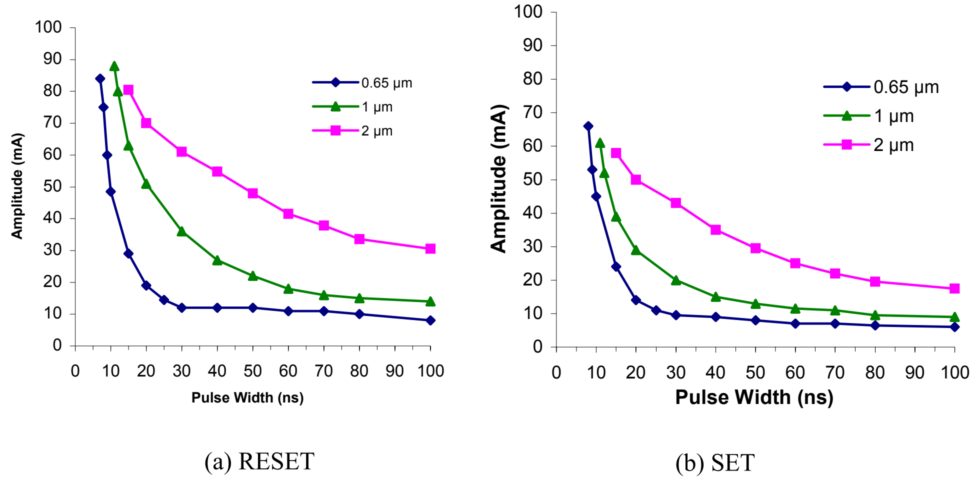


(a) (b)

Fig. 6 (a) R-I plot with crystalline background for CRAM with different dielectric layer 1 thickness, and (b) RESET programming current as a function of current pulse width

To study the scaling effect, CRAM memory cells with the same device structure and different feature size were fabricated. Figure 7 shows the programming current as a function of pulse width for memory cell with feature size of 2.0 µm, 1.0 µm and 0.65 µm, respectively. $Ge_2Sb_2Te_5$ is used as phase change material and was fixed at 50 nm. The results show that both RESET and SET programming currents highly depend on the feature size. Lower RESET/SET programming currents were obtained for memory cells with smaller size. In both RESET and SET graphs, the two pulse-dependent and independent regions can also be

observed for the three curves. It is interesting to observe that with the feature size shrinking, the independent region becomes wider and approaches to shorter pulse width.



(a) RESET (b) SET

Fig. 7 Programming current as a function of current pulse width for CRAM with different feature size (a) RESET and (b) SET states

4. Discussion

The exhibition of the two regions from the programming current versus pulse width curves is helpful for memory cell characterization. For practical usage, the pulse width independent region is preferred as short as possible. From our observation, the memory cells with lower programming current generally have short independent region.

The three I-W curves in figure 7 were fitted using equation (3), which contains the factor of feature size and repotted in Figure 8.

$$I = AI_0 + Be^{-\frac{C \bullet S}{D}} \qquad (3)$$

where, I is programming current; S is feature size; A, B, C and D are fitting constants which are size dependent. It can be seen that the fitting curves matches well with the experimental data.

Using the fitting method, we propose a new way to predict the RESET and SET programming current for memory cell. Applying the same fitting equation (3), the I-W curves for memory cell with small feature sizes were predicted and plotted in figure 8. From the fitting curves, it can be noticed that when the feature size reduces, the RESET and SET programming currents were reduced. At the same time, the pulse width independent regions were moved towards the short pulse width. The smaller the feature size is, the shorter the width-dependent region the curve has. In the pulse width dependent regions, the programming current required increases sharply when the pulse width reduces.

With this method, we can briefly predict and compare the performance of the memory cell with different structure, materials and feature size instead of experiments. For example, we can predict the RESET/SET programming current for memory cell with small size. From the fitting curves shown in figure 8, the RESET and SET programming currents required for memory cell with different feature size were extracted at different pulse width and depicted in Figure 9. The graphs show that the programming current scales with the feature size. The data in figure 8(a) suggest that the RESET currents for the memory cell with the above-mentioned cell structure and materials are about 0.9 mA and 0.4 mA for feature size of 180

nm and 45 nm, respectively. Besides the programming current, the programming speed can also be predicted from the graphs. For example, the data in figure 8(a) suggest that the shortest practical RESET pulse width for the memory cell with the above-mentioned cell structure and materials is around 20 ns when the feature size reduces to 45 nm. Figures 10 plots the pulse width vs. feature size when the programming current is fixed from the extract fitting data in Fig. 8.

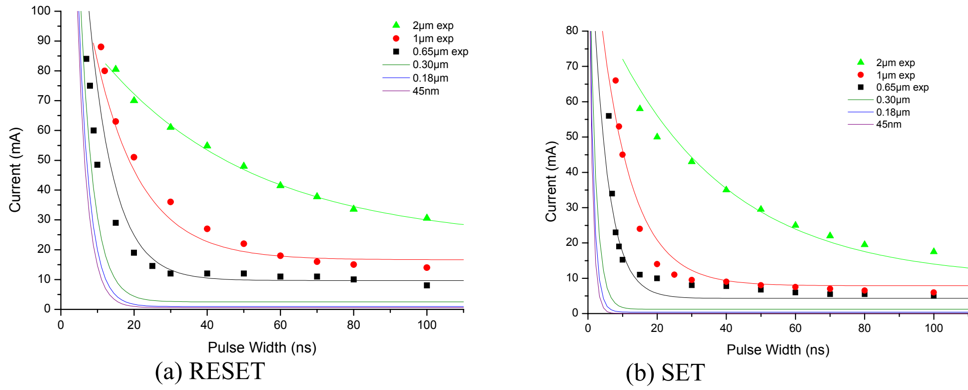


Fig. 8 Fitting curves for data in Fig. 7 programming current as a function of current pulse width for CRAM with different feature size (a) RESET and (b) SET states

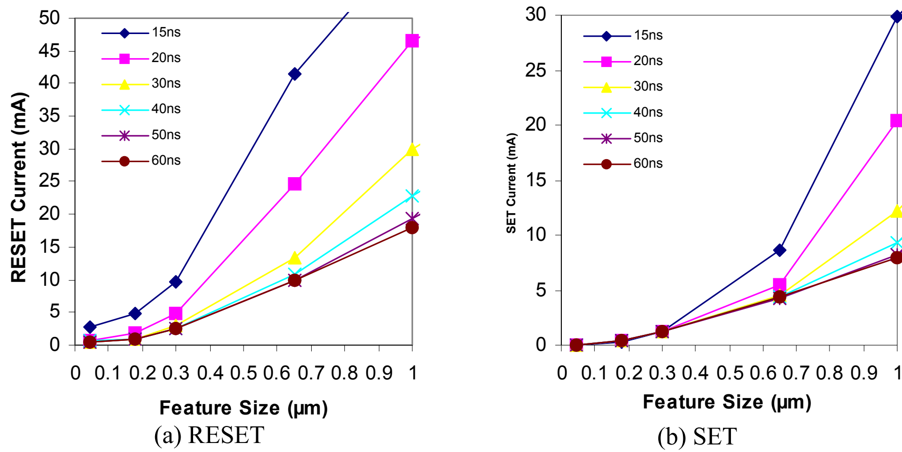


Fig. 9 Fix pulse width vs. feature size from the extract fitting data in Fig. 8 (a) RESET and (b) SET

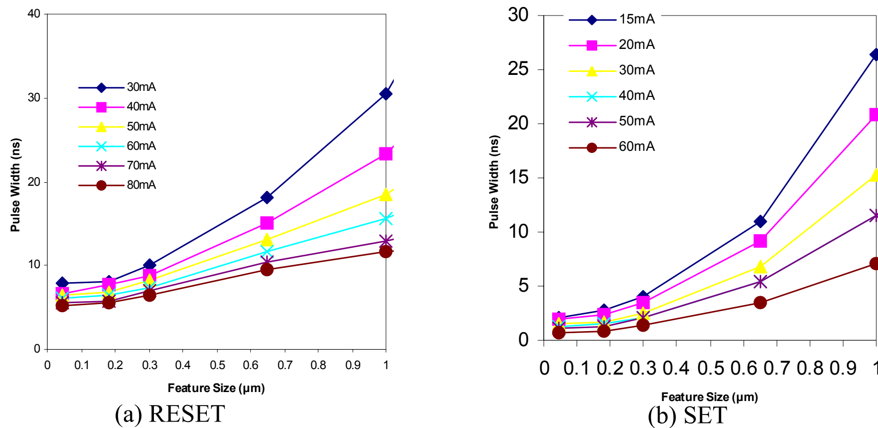
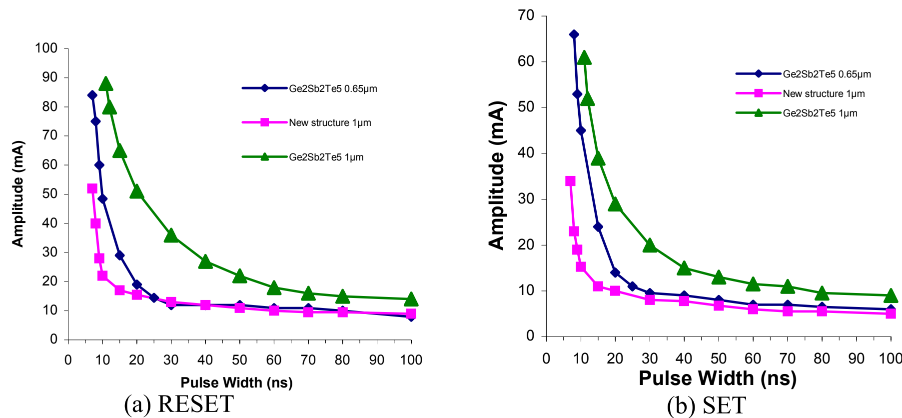


Fig. 10 Fix programming current vs. feature size extract from the fitting data in Fig. 8 (a) RESET and (b) SET

With the understanding from both simulation and experiments, a new structure phase change memory cell was proposed to reduce programming current. The memory cell with such structure have been fabricated with the feature size of 1.0 μm. Figure 11 gives the programmed current values of the SET/RESET states as a function of current pulse width. For comparison, CRAM memories with two different structures are fabricated. One has a $Ge_2Sb_2Te_5$ recording layer and the same feature size. Another has a $Ge_2Sb_2Te_5$ recording layer with a 0.65 μm feature size. All devices have the same recording layer thickness. The memory cell with the new recording structure has a wider relatively current independent region than the other two. The results show that the new recording structure reduces the programming current effectively. The RESET programming current has been greatly reduced about 70% and 25% for both SET/RESET with 15 ns pulse width compares to devices with single $Ge_2Sb_2Te_5$ recording layer with 1.0 μm and 0.6 μm feature size, respectively.



(a) RESET (b) SET

Fig. 11 Programming current as a function of current pulse width for CRAM with different structure (a) RESET and (b) SET

5. Conclusion

Through the simulation and experimental analysis, better understanding of the effect of different materials, cell geometry, structure, and feature size towards the CRAM cell performance has been obtained. It was observed that the RESET current is highly dependent on pulse width. Two regions, pulse-dependent and -independent regions were observed in the I-W curves. By fitting the I-W curves, we propose a new method to predict the performance of memory cell, e.g. RESET/SET programming current and programming width for memory cell. A new phase change recording structure is designed to reduce programming current. The memory cell with such new structure performs reduced programming current.

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