

# Material Selection through Band-alignment Study for PCRAM Integration

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## ABSTRACT

Tailoring the integration of PCRAM cell and logic device is important to achieve high density array. This work discusses about the impact of the interfaces of phase change material and surrounding materials on the integration by fundamental electronic studies. The energy band alignment of various phase change materials and electrode materials/isolating materials was investigated. The alignment would affect the carrier transport across the material interfaces: the carrier injection between electrodes and phase change materials and the carrier confinement between phase change materials with the isolating dielectric. The study provides a useful guidance to examine the interfacial properties and select suitable materials to optimize the PCRAM performances.

**Key words:** PCRAM, band alignment, carrier transport, integration

## 1. INTRODUCTION

Phase change random access memory (PCRAM) has gained increasing attention recently due to its near ideal non-volatile memory (NVM) characteristics, such as low power, high speed, high endurance, CMOS compatibility and high scalability [1]. It is based on the properties of chalcogenide-based phase change materials which can be reversibly switched between high resistive amorphous state and low resistive crystalline state by electric pulses. The high scalability and large ON/OFF resistance difference favoring for multi-level recording have enabled PCRAM as one of the most potential next generation NVMs. Currently 1 Gb PCRAM prototype based on 45 nm technology has been demonstrated [2].

However, to further increase the density of PCRAM, some hurdles are still need to be overcome, such as high RESET current, integration optimization, etc. The common approaches to increase density can be categorized into cell-level and array-level as shown in Table 1. At the cell level, scaling down the device feature size, reducing RESET current and achieving multi-level are the most efficient methods to increase density. Much efforts have been put on material and structure engineering of PCRAM to reduce current, such as to increase the thermal efficiency of the cell by doped phase change materials, novel heater, edge contact structure, confined structure, etc. [3-6]. At the array level, the cell and logic device integration and minimizing the cross-talk between cells are important. Meanwhile cross-bar architecture and 3D integration provide alternative solutions to further increase density. Thermal cross-talk has been investigated down to 16 nm [7]. It was found that isotropically-scaled devices, where all cell dimensions scale with the technology node, can be expected to experience no thermal crosstalk problems. The Damascene-GeSbTe cell process effect on the programming current was also evaluated [8]. It was found that the interfaces and its electrical and thermal properties are critical for power consumption. Interfaces reduce RESET power 20% and RESET current 40% and allow RESET current to scale faster than it would without interfaces. It was also found that the uniformity and controllability of the interface between phase change material and heater are critical for the optimized array integration.

Table 1 Common Approaches to Increase PCRAM Density

Cell	Scaling	Material and structure engineering
	Current reduction	
	Multi-level	
Array	PCRAM cell/logic device integration optimization	Cell efficiency, architecture
	Cross-talk minimization	
	Cross-bar architecture	
	3D integration	

With continuous size reduction of the PCRAM device, the importance of interfaces between materials becomes more evident. This work will discuss about the interfaces and material selection by fundamental electronic studies for PCRAM integration. Accurate knowledge of carrier transport at the interface between surrounding materials and phase change material could be necessary for further optimization of the device performance and to alleviate the RESET current requirement.

## 2. CONSIDERATIONS

Fundamental electronic studies on the energy band alignment between two materials would be a useful tool to examine the interfacial properties and its implications on device performances. The energy band alignment clearly affects the carrier transport across material interfaces, and provides insights into the physics at these interfaces in a PCRAM device.

Fig. 1 shows a generic PCRAM cell integrating with a logic device, highlighting the various interfaces in the structure. For instance, between an electrode and phase change material, the band lineups would affect the contact resistance and the injection of carriers between the two materials, thereby affecting the current and hence the programming current. However at the interface between a dielectric and phase change material, the valence band offset and conduction band offset would influence the carrier confinement in the phase change material region during device operation, thereby affecting leakage current, which has a larger impact on high density PCRAM array. Examination of the energy band alignment of phase change materials with the surrounding materials will enable the screening and evaluation of potential material candidates, even before integrating them into devices. The results achieved will provide a systematic guideline in the selection of suitable materials for implementation into future phase change memory devices.

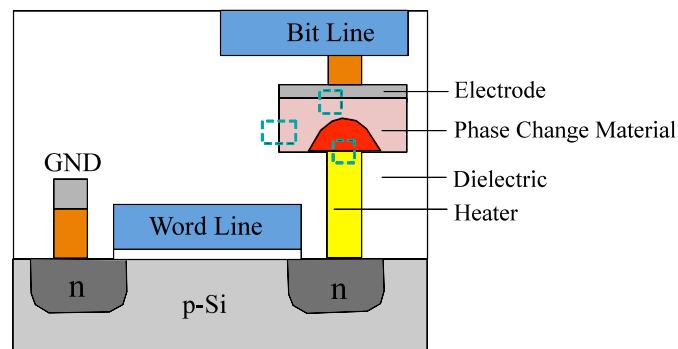


Fig. 1 Schematic drawing of a PCRAM cell integrating with a logic device

## 3. EXPERIMENTS AND RESULTS

High resolution x-ray photoelectron spectroscopy (HRXPS) was used to establish the band structure lineup between two materials, X and Y. The band alignment may be obtained by determining the valence band offset ' $\Delta E_v$ ' and conduction band offset ' $\Delta E_c$ ' between the two materials. In general, there are two methods available to determine the valence band offset between two materials. In the first method, the valence band offset can be simply inferred from

the difference between the valence band maximum energies of the two materials [9]. However, when two materials are put together, a dipole generally exists at the interface, which can account for 30 % of the valence band offset and thus cannot be neglected [10]. Therefore in the second method, the valence band offset was determined by consideration of a combination of both the valence band and core level spectra as it provides a more intricate insight of what happens at the interface. This technique has been widely exploited to determine the band offsets in a myriad of heterojunction systems, as well as the examination of the Schottky barrier height at metal-dielectric or metal-semiconductor interfaces.

A precise determination of  $\Delta E_V$  can be obtained by employing a technique reported by Kraut et al [11]. The core level energies at the interface are taken into consideration. Fig. 2 shows a schematic flatband diagram at the interfaces between two semiconductor materials X and Y, where  $\Delta E_V$ ,  $\Delta E_C$  and  $\Delta E_{CL}$  refers to the valence band offset, conduction band offset and core level energy difference at the interface, respectively.  $E_V$ ,  $E_C$ , and  $E_{CL}$  are the valence band minimum, conduction band maximum and core level binding energies, while “(i)” represents the core level binding energy at the interface between the two materials. The bandgap of the materials is denoted by  $E_g$ . The Fermi level ( $E_F$ ) is employed as the reference level, where binding energy ( $E_B$ ) is taken to be zero.

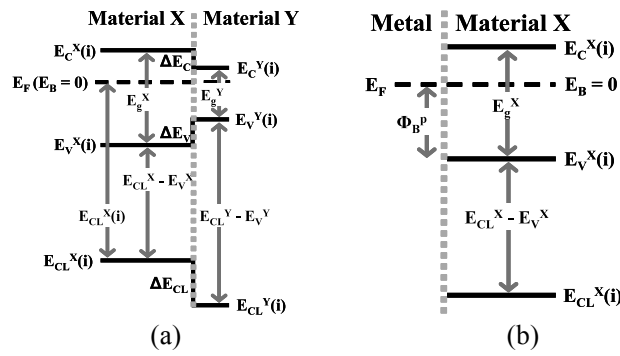


Fig. 2 Schematic flatband diagram for the band line-up (a) at the interfaces between two semiconductor materials, X and Y and (b) at a metal/ semiconductor interface.

The governing equations for determination of the valence band offset and conduction band offset between two materials, as well as the hole barrier height,  $\Phi_B^p$ , measured by XPS are illustrated in equations (1) – (3),

$$\Delta E_V = (E_{CL}^Y - E_V^Y) - (E_{CL}^X - E_V^X) - (E_{CL}^X(i) - E_{CL}^Y(i)), \quad (1)$$

$$\Delta E_C = E_g^X - E_g^Y - \Delta E_V, \quad (2)$$

$$\Phi_B^p = E_V^X - E_{CL}^X + E_{CL}^X(i), \quad (3)$$

where the notations have already been described in the previous paragraph.

Material studies based on HRXPS analysis was performed on blanket samples. For precise determination of the valence band offset, bulk samples of both of the investigated materials, as well as an ultrathin overlayer of one material over the bulk films are required, in order to probe the core level energies of both materials near the interface.

The conduction and valance band offset of various phase change materials and surrounding dielectric and metal materials have been studied. Table 2 summaries the offset of phase change materials with different dielectric materials [12-14]. It can be seen that the valence band and conduction band offsets were found to vary with the composition of  $\text{Ge}_x\text{Sb}_y\text{Te}_z$ . It illustrates that the choice of phase change materials impacts the energy band offsets. However, the impacts are not as high as the choice of dielectric materials. The data shows that the band offsets of phase change materials and dielectric are highly affected by the type of the dielectric materials. In Table 2,  $\text{SiO}_2$  provides the largest barrier height between phase change materials which shows it would be a good choice for isolating the PCRAM cell with neighboring cells with less leakage path in the surrounding dielectric layers.

Table 2 Conduction and Valance Band Offset of Various Phase Change Materials and Dielectric Materials [12-14]

		Sb <sub>2</sub> Te <sub>3</sub>	Ge <sub>1</sub> Sb <sub>4</sub> Te <sub>7</sub>	Ge <sub>1</sub> Sb <sub>2</sub> Te <sub>4</sub>	Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub>	GeTe	N-Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> (3.5%)	N-Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> (6.2%)	N-Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> (7.7%)
SiO <sub>2</sub>	$\Delta E_c$	3.28	3.04	2.98	2.79	3.33	3.37	3.49	3.4
	$\Delta E_v$	5.15	5.21	5.26	5.36	4.82	4.8	4.5	4.4
Si	$\Delta E_c$				0.32				
	$\Delta E_v$				0.1				
HfO <sub>2</sub>	$\Delta E_c$				1.2				
	$\Delta E_v$				2.9				
Si <sub>3</sub> N <sub>4</sub>	$\Delta E_c$				2.8				
	$\Delta E_v$				1.9				

The offset of phase change materials and different electrode materials was also investigated [15]. It was observed that a higher work function metal gives rise to a more negative hole barrier. The hole barrier height is the difference between the Fermi-level of the metal and the valance band of the phase change film. Significant Fermi level pinning effect to the charge neutrality level at the interfaces of phase change material was found. Good ohmic contact can be achieved even with a low work function metal. This suggests that there are a large range of metals for good contacts on phase change films. However, although good ohmic contact could be achieved by various metals, the difference in the hole barrier height can be used as a guide to select a better electrode material for PCRAM application. GeSbTe chalcogenide materials are reported to be p-type materials. Hence, lower hole barrier height is possible to reduce the contact resistivity between the metal and phase change materials and gives a higher current for Joule heating in the phase change layer for a given bias. It is observed that increasing the nitrogen content in the phase change film generally raises the hole barrier height, while increasing the vacuum work function of the metal adjacent to the phase change films results in a more negative hole barrier height. The observation would provide a guideline to screen the electrode materials for low current operation from the point of view of efficient electron transportation.

### 3. CONCLUSION

The electron transportation at the interfaces between phase change materials and surrounding materials is investigated through the band alignment study. The offset between the electrode and phase change materials affects the contact resistance and the carrier injection, which affects the current consumption. While the offset between surrounding dielectric and phase change material influences the carrier confinement in the phase change material region, which affects the leakage current for high density array integration. The study on band alignment has provided a useful tool and guidance to select suitable materials for integration optimization.

### REFERENCES

1. R. Bez: "Chalcogenide PCM: a Memory Technology for Next Decade", IEDM Tech. Dig. (2009).
2. G.Servalli: "A 45nm Generation Phase Change Memory Technology", IEDM Tech. Dig. (2009).
3. H. Horii, J. H. Yi, J. H. Park, Y. H. Ha, L. G. Baek, S. O. Park, Y. N. Hwang, S. H. Lee, Y. T. Kim, K. H. Lee, U-I. Chug, and J. T. Moon: "A Novel Cell Technology Using N-doped GeSbTe Films for Phase Change RAM", Symp. VLSI Tech. Dig. (2003).
4. N. Takaura, M. Terao, K. Kurotsuchi, T. Yamauchi, O. Tonomura, Y.Hanaoka, R. Takemura, K. Osada, T. Kawahara, and H. Matsuoka: "A GeSbTe phase-Change Memory Cell Featuring a Tungsten Heater Electrode for Low-Power, Highly Stable, and Short-Read-Cycle Operations", IEDM Tech. Dig. (2003).
5. Y.H. Ha, J.H. Yi, H. Horii, J.H. Park, S.H. Joo, S.O. Park, U.-I. Chung and J.T. Moon: "An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption", Symp. VLSI Tech. Dig. (2003).
6. J. I. Lee, H. Park, S. L. Cho, Y. L. Park, B. J. Bae, J. H. Park, J. S. Park, H. G. An, J. S. Bae, D. H. Ahn, Y. T. Kim, H. Horii, S. A. Song, J. C. Shin, S. O. Park, H. S. Kim, U.-I. Chung, J. T. Moon and B. I. Ryu: "Highly Scalable Phase Change Memory with CVD GeSbTe for Sub 50nm Generation", VLSI Symp. Tech. Dig. (2007).

7. U. Russo, D. Ielmini, A. Redaelli, and A. L. Lacaita: "Modeling of Programming and Read Performance in Phase Change Memories - Part II: Program Disturb and Mixed-scaling Approach", *IEEE Trans. Electr. Dev.*, 55(2), 515, (2008).
8. D. L. Kencke, I. V. Karpov, B. G. Johnson, S. J. Lee, D. C. Kau, S. J. Hudgens, J. P. Reifenberg, S. D. Savransky, J. Zhang, M. D. Giles, G. Spadini: "The Role of Interfaces in Damascene Phase-Change Memory", *IEDM Tech. Dig.* (2007).
9. H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D.-L. Kwong, J. S. Pan, C. H. Ang, J. Z. Zheng, and S. Ramanathan, "Energy Gap and Band Alignment for  $(\text{HfO}_2)_x(\text{Al}_2\text{O}_3)_{1-x}$  on (100) Si," *Appl. Phys. Lett.*, 81, 376, (2002).
10. W. Monch, "On the Electric-dipole Contribution to the Valence-band Offsets in Semiconductor-oxide Heterostructures," *Appl. Phys. Lett.*, 91, 042117, (2007).
11. E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk, "Precise determination of the valence band edge in x-ray photoemission spectra: Application to measurement of semiconductor interface potentials," *Phys. Rev. Lett.*, 44, 1620, (1980).
12. L. W.-W. Fang, J.-S. Pan, R. Zhao, L. P. Shi, T. C. Chong, G. Samudra, and Y.-C. Yeo: "Band Alignment between Amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and Prevalent Complementary-metal-oxide-semiconductor Materials", *Appl. Phys. Lett.* 92, 032107 (2008).
13. L. W.-W. Fang, Z. Zhang, J.-S. Pan, R. Zhao, M. H. Li, L. P. Shi, T. C. Chong, and Y.-C. Yeo: "Dependence of Energy Band Offsets at  $\text{Ge}_2\text{Sb}_2\text{Te}_5/\text{SiO}_2$  Interface on Nitrogen Concentration", *Appl. Phys. Lett.* 94, 062101, (2009).
14. L. W.-W. Fang, R. Zhao, Z. Zhang, J.-S. Pan, L. P. Shi, T. C. Chong, and Y.-C. Yeo: "Band offsets between  $\text{SiO}_2$  and phase change materials in the  $(\text{GeTe})_x(\text{Sb}_2\text{Te}_3)_{1-x}$  pseudobinary system", *Appl. Phys. Lett.* 98, 132103, (2011).
15. L. W.-W. Fang, R. Zhao, J.-S. Pan, Z. Zhang, L. P. Shi, T. C. Chong, and Y.-C. Yeo: "Fermi-level pinning at the interface between metals and nitrogen-doped  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  examined by x-ray photoelectron spectroscopy", *Appl. Phys. Lett.* 95, 192109, (2009).

## Biographies

Zhao Rong received her Ph.D. degree in electrical and computer engineering from National University of Singapore in 1999 with a topic on application of low-temperature GaAs quantum well laser on Si substrate. In 1998, she joined the Optical Media group in Data Storage Institute, Singapore, where she was involved in the development of high density re-writable optical disk. Since 2002 she has been working on the development of phase change random access memory (PCRAM). Currently she is a senior research scientist and program leader of PCRAM/RRAM. Her research interest also include artificial cognitive memory.